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SEPTEMBER 30, 1985

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PAGE 46

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MAINFRAME TECHNOLOGY SPEEDS UP CAE WORK STATION/54

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SEPTEMBER 30, 1985 VOLUME 58, NO. 39

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PUBLISHER'S LETTER

In this issue of *Electronics* is the first appearance anywhere in our industry of a service that will give our readers information, at several levels of detail, about applications and features of advertised products. While advertisers have customarily used some combination of local sales offices, direct phone lines, toll-free 800 numbers, and reader-service numbers in their advertisements to provide such data, none satisfactorily provides rapid access to detailed information.

Now, that problem appears to be solved. We are making available an information-retrieval service called Kwik/Quest that was developed by Tallant-Yates Advertising Inc. of Englewood, Colo. Its first use, with an advertisement from Hewlett-Packard Co. for its HP 9000 series 300 computer, is on p. 23.

Anyone with access to a computer and a modem may use Kwik/Quest to obtain tightly focused, problem-specific responses to his or her questions. Kwik/Quest uses a logical-tree structure to access data sheets, user documentation, and system documentation. And thanks to a combination of sophisticated indexing and cross-referencing with elements from expert-systems technology, information-handling theory, and task documentation writing, Kwik/Quest's database users can move quickly from problem to solution. In fact, the reader can request in-person product demonstrations or specific application information, or even purchase the product while still connected to the system.

One of the most useful features of the service is its accessibility: the user can log on to it seven days a week, 24 hours a day, so that work hours or sales-office hours are no problem. This effort to bring reader-advertiser communications into the high-tech age can only benefit us all.

Speaking of electronics and communications, our article on p. 36, "Australians has major doubts over its high-tech prowess," serves as a good practical illustration of how communications technology has served to shrink the globe.

When we asked Craig Addison, editor of *Australian Electronics Engineering*, to provide our readers with a look at the electronics industry in his country, we were a little bit nervous about moving words, pictures, and illustrations across some 8,000 miles, not to mention the International Date Line. Although we routinely accomplish this when working with our Tokyo bureau, that routine has been refined over the many years we have had that link.

Nevertheless, we can now report that communications with the Southwest Pacific are flawless. Telephone connections between the U. S. and Sydney, Australia—where Craig has his office—were swift and clear, and Telex service was equally efficient.

Aside from the 16-hour time difference between New York and Sydney, as well as other minor dislocations—for example, associate managing editor Howard Wolff, who handled the story in New York, reports missing two touchdown plays on Thursday Night Football while he was on the telephone with Addison—all went well, as you can see.

Laurence Altman

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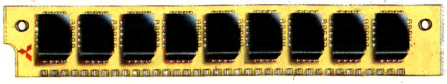

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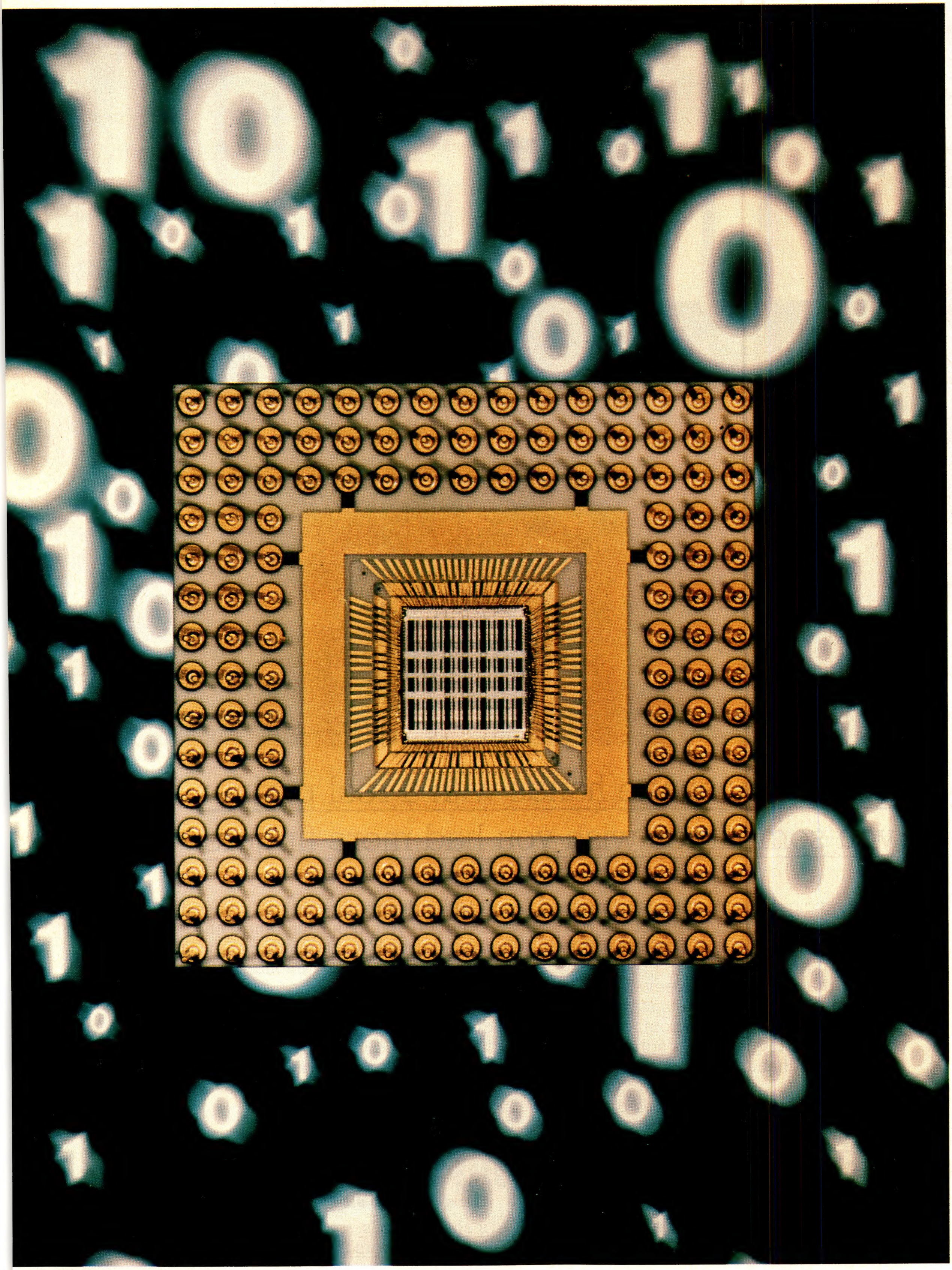

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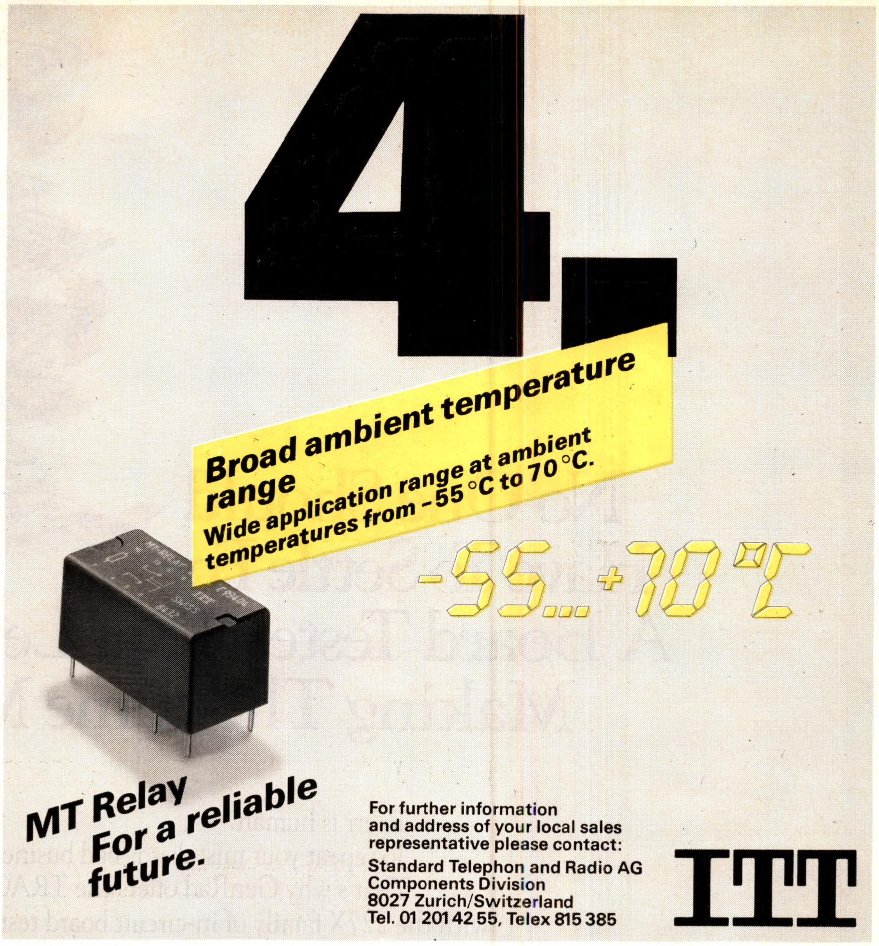

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Electronics October 28 issue

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Technology Update: Manufacturing

Robots in plant automation, the integration of non-manufacturing functions, and other innovations are revolutionizing manufacturing. Downloading inventory, cost, and design information (computer-integrated manufacturing) is becoming standard. This report examines the newest techniques in the most advanced plants.

The Market
$17.6 billion in 1985; $19.2 billion in 1986.

Target Readers
Plant managers and others involved in automating factories; marketing managers for makers of automation equipment and networks for computer-integrated manufacturing.

Issue Date:
October 28, 1985

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Electronics
Influence Beyond Design

ELECTRONICS NEWSLETTER

EVER-OPTIMISTIC CHIP MAKERS EXPECT 'DRAMATIC TURNAROUND' IN 1986

The semiconductor slump has nearly run its course, and the industry will resume its long-term growth next year—if the new forecast of the World Semiconductor Trade Statistics program can be believed. Next year will see a "dramatic turnaround" in sales that will just about make up for this year's severe decline, according to estimates made at last week's annual forecast dinner of the Semiconductor Industry Association. Worldwide sales, which will slump this year to about $21.6 billion from 1984's record $25.9 billion, will rebound and grow at an 18% rate to $25.4 billion in 1986. The 1988 forecast is even rosier, with sales expected to reach $38.4 billion. The group says excess inventories—which it blames for the 1985 disaster—are nearly burned off. Bullish forecasts are nothing new for the cooperative trade program, which is run by a committee from the SIA, the Electronics Industries Association of Japan, and the European Electronic Component Association. Last September, the group predicted record 1985 sales of $32.3 billion, a figure that it has been revising downward ever since. Worst hit by this year's 1985 slump is the U. S., which will show a drop in 1985 sales of 28.7%, far deeper than the drops of 4.5% in Europe and 6.4% in Japan. □

IBM OUT TO BUILD A STRONGER POSITION IN JAPAN WITH NTT PACT

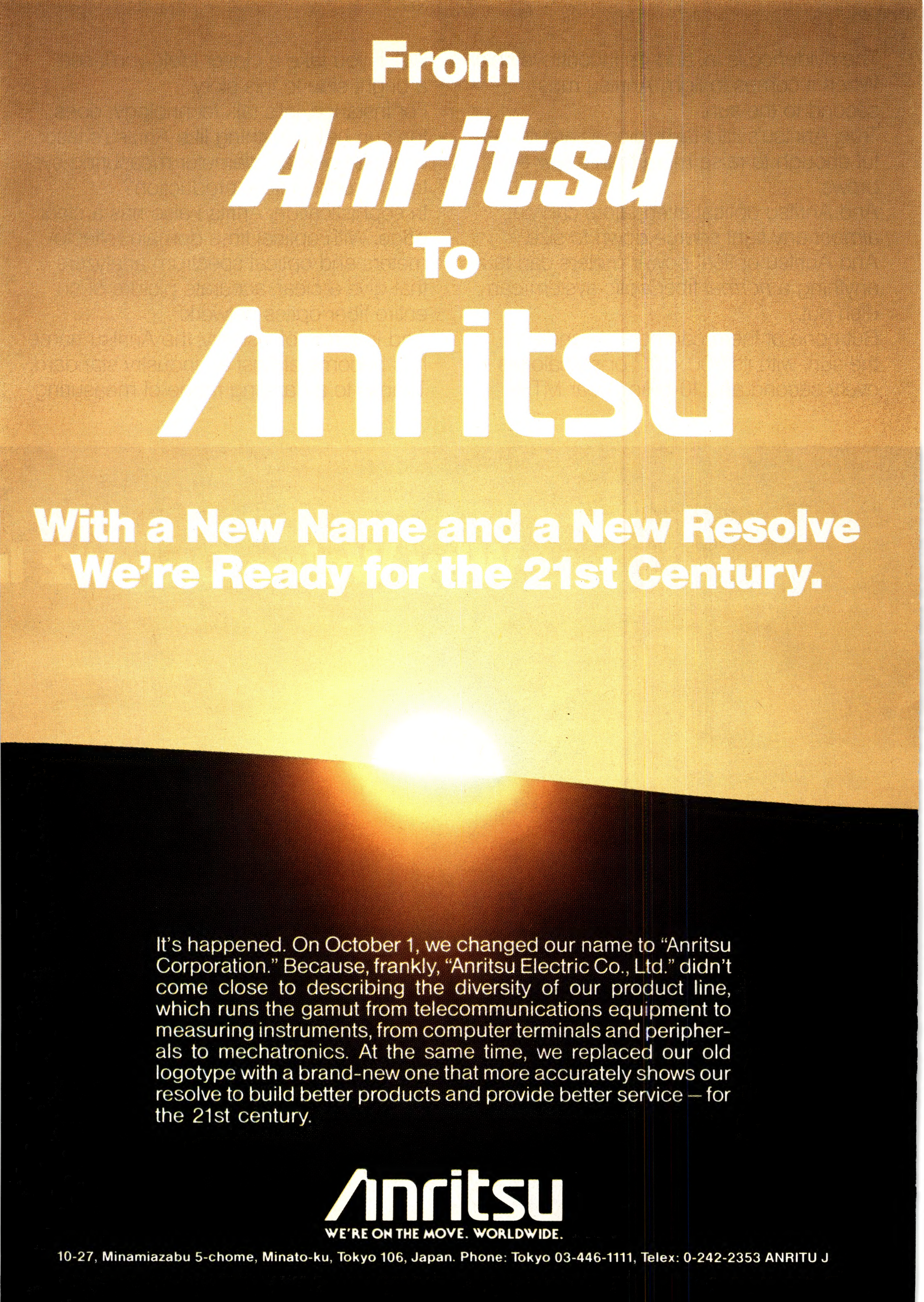
IBM Corp.'s strategy to position itself more strongly in Japan, the world's No. 2 computer market, got a shot in the arm last week when IBM Japan Ltd. and Nippon Telegraph & Telephone Corp. formed a long-expected joint venture to market a protocol package for standard data communications services, which links IBM's Systems Network Architecture with NTT's Data Communications Network Architecture (DCNA). The as-yet-unnamed joint company will be capitalized at close to $2.7 million, with a staff of between 50 to 60 people. Operations, which will begin early next year, will also include value-added network (VAN) services. Industry analysts noted that the IBM-NTT deal also helps the computer maker counter AT&T Co., which last July joined a group of Japanese companies to form a VAN venture in Japan. □

JEDEC STALLS ON MEGABIT CHIP-PACKAGING STANDARDS

With megabit dynamic random-access memories ready for sampling (see story, p. 30), a growing number of the members of the Joint Electron Device Engineering Council's 43.2 memory panel doubt that Jedec will have any influence over the packaging standards. Efforts to set dimensions of packaging profiles for 1-Mb DRAMs seem more at an impasse than they were six months ago. The controversy continued during the September meeting of the 43.2 memory panel. Earlier this year, a straw vote narrowly passed a 300-mil-wide small-outline J-leaded package, backed by Texas Instruments Inc. Several producers who agreed to back this package now worry about the 300-mil width. They fear problems with long, narrow chips and thin plastic protection of megabit silicon. A task group will meet twice on the issue before the December 43.2 meeting in San Diego. □

VECTRA IS HP'S FIRST IBM PC COMPATIBLE

Bowing to the inevitable, Hewlett-Packard Co. last week joined the ranks of manufacturers offering computers compatible with IBM Corp.'s Personal Computer. The PC AT-compatible Vectra uses the 8-MHz version of Intel Corp.'s 80286 microprocessor, which lets it run programs 30% faster than the PC AT. Color display resolution is 640 by 400 pixels, about twice the resolution of the PC AT. An entry-level system with 256-K of main memory and one 360-K 5¼-in. disk drive, costs $3,199. □



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As of October 1, 1985, Anritsu Electric Co., Ltd. became Anritsu Corporation.

products are where you should make money. What we have done is put in place the vehicle for a broader range of noncommodity chips," he says, responding to concerns that TI's EPROM introduction is an entry into yet another turbulent market. Benefits from the EPROM work will likely first show up on a new CMOS 8-bit microcontroller under development. TI also hopes to use the technology to produce CMOS field-programmable logic, new electrically erasable PROMs, low-power linear products, and "smart" power ICs.

Like competing high-density EPROMs already on the market, TI's chips use a programming algorithm that speeds up the writing of software into the 256-K nonvolatile memories from as much as 6 minutes to a typical 132 seconds. Read-access time is 170 ns. From the same HVCMOS technology, the company plans to soon add 64-K and 512-K chips to the EPROM product line, offering access speeds comparable to the market standards. However, TI is working on an advanced version of HVCMOS that could result in faster, less power-hungry EPROMs, using silicides to lower interconnect resistance. *–J. Robert Lineback*

BUSINESS

IS THE THIRD QUARTER THE LOW MARK FOR ICs?

NEW YORK

As semiconductor executives scratch their heads and scan the entrails of chickens in attempts to augur the future of their industry, they agree on one thing: business in the just-ended third quarter probably hit the low point in the current recession.

An upturn in semiconductor shipments is not imminent, despite the indefatigable optimism of industry trade associations (see p. 11). Most executives and industry watchers still speak of low inventory levels at customer sites as a reason why business should improve soon, as if to indicate that things can't stay bad forever. But nothing is being taken for granted.

"Until we experience a sustained improvement in booking rates, business will continue to be very difficult," says Gary Arnold, vice president of finance for National Semiconductor Corp., Santa Clara, Calif. Semiconductor executives will probably be very happy when the third quarter is behind them, says Jack Beedle, president of In-Stat Inc., a market-research company in Scottsdale, Ariz. He says the industry will register worse losses for the quarter than in any other three-month period in history.

Echoing these feelings, Michael Stark, an analyst with investment bankers Robertson, Colman & Stephens in San Francisco, notes that "no large semiconductor company will have operating profits from their semiconductor operations" in the third quarter.

Earlier this month, for example, National Semiconductor disclosed that it had already lost $44.3 million in the first quarter (excluding the results of its National Advanced Systems unit), though sales for the first half of the period were only $175.7 million. Some industry analysts think National could lose as much as $50 million to $60 million in the third quarter.

And Advanced Micro Devices Inc., Sunnyvale, Calif., had operating losses of $14.5 million for the quarter ended last June, though it showed a profit for the quarter of $700,000 because of a tax credit. This quarter, "our losses will be larger," a spokesman says.

In-Stat predicts third-quarter U. S. and worldwide chip sales will drop between 8% and 9%. The industry has now had five consecutive quarters of business declines, but it will likely see an end to the fall in the fourth quarter, for which In-Stat forecasts a slight 3% to 4% dollar-volume rise due to traditional scrambles to clear out vendor backlogs.

"We'd like to think there will be an upturn in the first quarter," says John Stratford, merchandising manager of NCR Corp.'s Microelectronics Division in Dayton, Ohio. "But we have seen very little evidence that it's going to happen.

"My own personal belief is that we'll see some small upturn in the first quarter and that the remainder of 1986 should see some quarter-by-quarter growth. But it's going to be a pretty slow year in 1986, I think. If anything, it will only be a few percentage points over the previous year."

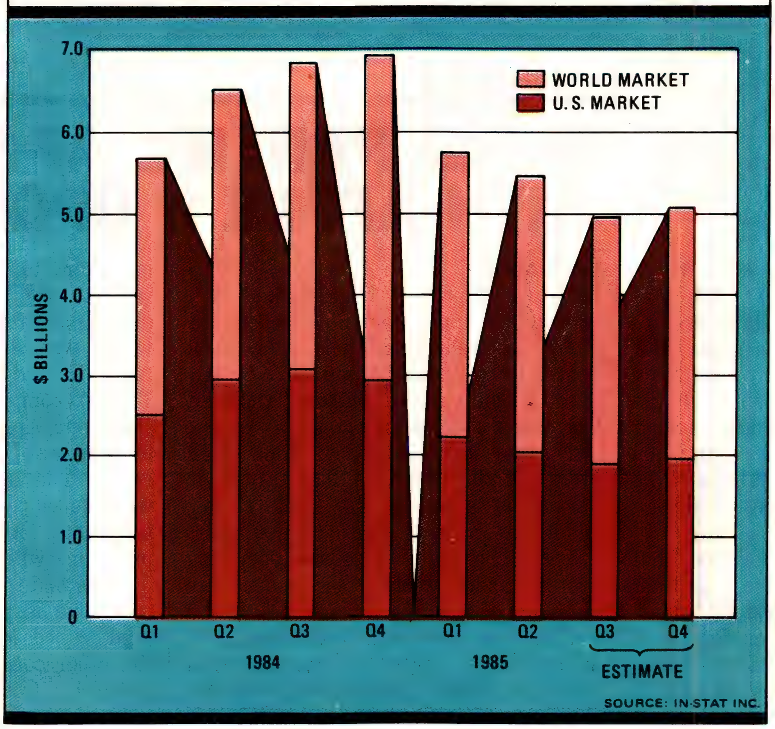
TRICKLE OF ORDERS. There is some evidence that orders are starting to trickle in, according to James L. Barlage, an analyst at Smith Barney Harris Upham & Co., New York. "The small- and mid-size users, the ones who couldn't build inventory up as high as the larger customers, are back in the market placing very small, short-term types of orders." Some larger companies also are starting to place small orders, he adds.

But Barlage sees a repeat of 1982's first quarter, when a large influx of orders following the 1980-82 recession falsely indicated an industrywide boom. "There will be an aborted recovery in the first quarter of 1986. Orders will build up and then tail off [because] the economy won't come through strong enough" to sustain a chip-business upturn, he says.

Order rates for the industry have stopped plunging, and shipments by distributors—who generally feel business trends five to six months before manufacturers—have risen slightly, notes Charles M. Clough, president of Wyle Laboratories' Electronics Marketing Group in Irvine, Calif.

One reason for losses by semiconductor companies is too much capacity, says industry consultant Matt Crugnale of Crugnale & Associates, Mountain View, Calif. "Somewhere along the line, the volume

SEMICONDUCTOR SALES COULD BOTTOM OUT IN THE THIRD QUARTER



SOURCE: IN-STAT INC.

memory comes in 128-K-byte increments, up to 640-K bytes for the IIc and 1.5 megabytes for the IIe. The price, with a 256-K-byte RAM card, is about $480. The company claims that the IIc upgrade, with its 640-K bytes of RAM, makes the system run four times faster.

The boards run under Micro Magic's MAX-OS multiuser, multitasking, Unix-like operating system. MAX-OS lets the system take advantage of its 8- and 16-bit microprocessors.

Micro Magic wrote MAX-OS to run its own 16-bit upgrade board, the MAX-816, which company president Will Troxell says costs $495 base price, addresses 16 megabytes of RAM, "runs cool as a cucumber, and runs circles around an IBM PC." The MAX-816 has its own external power supply, so it can tap all 16 megabytes of memory, and is not limited by the power supply of the system.

Troxell says Micro Magic is aiming for the higher end of the upgrade market. The company will eventually introduce 65C816-based products that will transform the Apple II computers into $10,000 work stations running at 6 MHz with high-resolution graphics and a fast disk controller.

Troxell and his partner, Frank Krol, have worked closely with the designer of the 65C02 and the 65C816, Bill Mensch, of Western Design Center in Mesa, Ariz., to design the MAX operating system. All believe the operating system itself may become as ubiquitous as did the CP/M operating system for machines based on Zilog Corp.'s Z80 8-bit microprocessor.

HIGHLY VERSATILE. "My goal is to make it the MSX/MS-DOS-whatever-else of the USA," says Troxell. Its present version is written specifically for Mensch's chip, but Troxell says it is written mostly in the C language—known for its ease of movement among machines—with few assembly-language drivers. "It could be written and compiled with just about any computer's C compiler, and probably would work with most anything."

The 40-pin CMOS 65C816 has 16 megabytes of address space, compared with 64-K bytes on the 6502. (The power supply of the IIe and IIc limits memory capacity to 1.5 megabytes internally.) It has new outputs, called valid program addresses, for dual-cache memory handling. An abort input allows virtual-memory systems to be built, and a new wait-for-interrupt instruction allows for higher-speed input.

Mensch says the on-board 8-bit emulation for existing software was an obvious feature. "A brand-new 16-bit microprocessor coming out right now wouldn't have much chance of success in the market when people are delivering 32-bit processors," he says. "But because it runs all the old software with no changes, I could state with a fair degree of accuracy that I have more software running on my microprocessor than Motorola has on the 68000," the chip used on the Apple Macintosh.

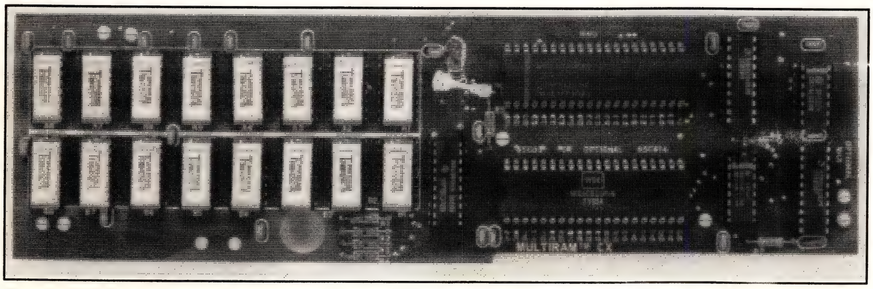
Checkmate president Andy Niemic says Apple isn't interested in designing for the retrofit market. Instead, he claims Apple may want to sell his board—aimed at a less professional market than Troxell's—through dealers.

Apple's own upgrade of the II isn't slated to appear until 1986

Apple would not speculate on such strategies, saying only that its new attitude toward third-party developers has it talking to many vendors. But an Apple representative says that "as far as a game plan, we plan to bring the 2.5 million [installed user base] along with us."

COUNTING ON APPLE. Both Niemic and Troxell are banking on Apple including the 65C816 in that strategy. Niemic claims software developers are using his board, not emulations, to write programs for Apple's coming II upgrade. . "You're never sure about compatibility in these situations, and Apple only gives you information on a need-to-know basis," he says. "So we gave all the developers we could find a board so they could feel better about writing compatible software."

Western Design Center has been shipping production quantities of the 65C816 for four months. Mensch says he delivered first samples to Apple in March of 1984, but won't say if Apple has ordered production quantities. *–Denise Caruso*



CARD CHIP. Checkmate's Multiram interface card carries the 65C816 chip, which addresses 16 megabytes of memory, with an abort input to allow building of virtual-memory systems.

COMPANIES

TEKTRONIX SUFFERS DESPITE PLANNING

NEW YORK

Planning for a business downturn can ease a company's losses or dip in profits, but when that downturn is more severe than expected, it adds an extra jolt. That's the problem that Tektronix Inc. ran into in its first fiscal quarter, which ended Aug. 24. "The plan we put together for fiscal 1986 had a poor first quarter structured into it," president Earl Wantland told a meeting of securities analysts last week. "But the quarter was worse than we expected."

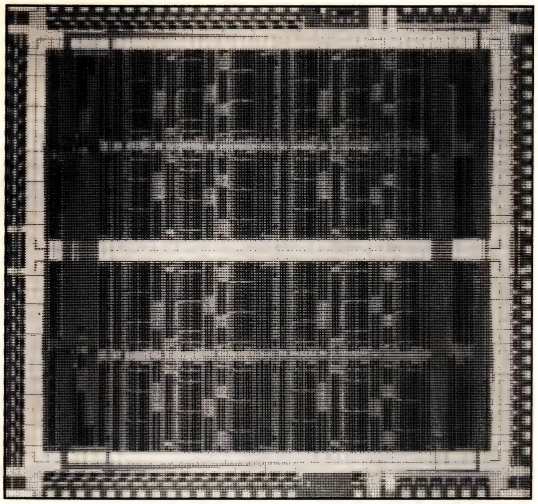
Tektronix couldn't cut its expenses quickly enough to cope with the unanticipated drop in business, company executives pointed out. In addition, its orders included a higher-than-expected percentage of low-margin products. The company's earnings were further reduced by $3.8 million when it decided to get out of the proprietary computer-aided-engineering work-station market (see p. 61).

As a result, Tektronix earned just $3.5 million in the first quarter compared with $16.2 million a year ago. Sales slipped to $302.5 million from last year's $307 million. "We really are off to a sluggish start," said senior vice president and chief financial officer Larry N. Choruby.

"If the business climate holds up and orders hold up, there's no reason we won't make our profit plan for fiscal 1986," said Willem B. Velsink, executive vice president of the Beaverton, Ore., company. "At this point, we have no reason to be pessimistic, but we have to be realistic." This realism reflects the fact that the worldwide market for Tektronix's products has slowed in growth, he said. The industrial sector in the U.S. and Europe is flat, he said, and Japan's economy is slowing.

TRIMMERS READY. If business doesn't pick up, Tektronix stands ready to further trim its corporate expenses. One economy move is to freeze hiring (the company currently is hiring only new college graduates). The company also is considering increasing attrition by not replacing most of the 75 people who leave the company every month, and subcontracting work.

Tektronix is fighting back against the downturn by putting its money on the line for new products. Wantland noted that the company invested 13% of its sales in research and development in fiscal 1985, the highest percentage of sales since 1947. The company, which traditionally invests 10% of sales in research and development, is continuing with the



MANY SIMPLE GATES. Multiplier IC for fast Fourier transform was built from 10,800 simple logic gates on a 268-by-289-mil chip.

cells that the company calls Supracells.

Thus the multiplier IC was built from 10,800 simple logic gates. It fits onto a chip measuring 268 by 289 mils and is packaged in a 120-lead pin-grid array.

Large blocks turn up in the butterfly chip. It performs addition or subtraction for one channel of one stage—or rank—of the pipelined FFT, switching between real and imaginary channels under chip control. The needed delay or data reordering is accomplished by a small 256-by-16-bit RAM controlled by a counter.

A ROM that stores 512 12-bit words is also incorporated on the chip. The ROM holds the complex coefficients used as one of the terms in the multiplier chip.

The majority of the data path is implemented in three automatically routed gate arrays. The control section is made up of standard low-level logic cells. The ROM and RAM structures are generated automatically from the Megacell library. All told, the butterfly chip has 5,500 gates, 4-K bits of RAM, 6-K bits of ROM, plus a 64-by-9-bit test-control NAND PLA. The chip measures 263 by 317 mils and is also packaged in a 120-lead pin-grid array.

Plessey incorporated self-testing circuitry on the FFT chips because their complexity would have made conventional production-line testing difficult. Eventually, says Fox, Plessey hopes to add self-test structures to the Megacell library. *–Kevin Smith*

PERIPHERALS

ERROR-CORRECTION CHIPS BOOST OPTICAL STORAGE

COLORADO SPRINGS

Optical memory disks have such high bit density that optical-storage drives are severely constrained by media defects. That spells problems for makers of write-once and erasable-disk drives, but opens the door for a new class of integrated circuits for error detection and correction. At least one company has already begun delivery of a chip for optical-storage drives, and two others expect to have products within 90 days.

The appearance of the error-correction chips heralds a scramble for market position as drive makers ready the first generation of write-once optical drives [*Electronics*, Sept. 16, 1985, p. 26]. Two such drives have already been introduced and more than a score are expected within a year. Early indications are that they will all use different proprietary error-correction schemes. The inevitable result, many believe, will be a struggle to impose a de facto standard on the industry.

All three of the new chips use Reed-Solomon coding, a form of error correction that operates by generating a polynomial whose coefficients are binary data symbols and whose exponents are positional indicators for a given data block. The polynomial is decoded for error locations by an algorithm that performs Galois field algebra.

Although the approaches are similar, the chips differ in the length of their Reed-Solomon codes and the algorithms that accompany them. They all, however, must contend with a raw-error rate—number of error events divided by the number of bits transferred—on the order of 10^{-4}, and correct it to 10^{-12} in order to satisfy the demands of write-once and erasable drives.

First to claim a working error-correction chip is Design Engineering Inc., of Boulder, Colo., a design house that specializes in semicuston chips using the NCR Corp. cell library and NCR's CMOS foundry in Ft. Collins, Colo. Design Engineering's production is going to Information Storage Inc. of Colorado Springs, one of the first two companies to hit the market with a write-only optical drive. Eventually, however, Design Engineering will offer the chip for other optical and even magnetic drives.

The maker of the only other currently available 5¼-in. write-once drive is Optotech Inc., also of Colorado Springs. Optotech uses a board running an error-correction algorithm developed by Neal Glover of Data Systems Technology, Broomfield, Colo.

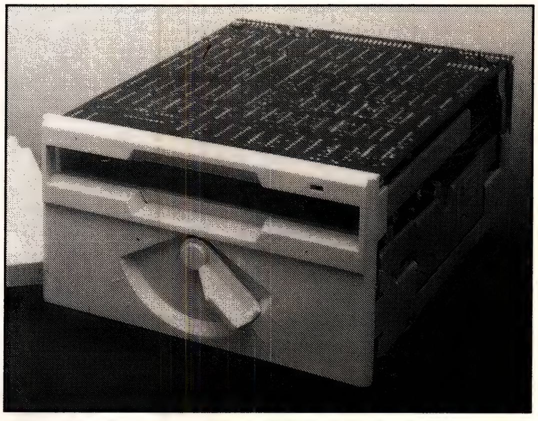
Glover, author of a text on error correction for engineers, is designing a chip around his algorithm. He has formed an alliance with Scientific Micro Systems Inc., of Mountain View, Calif., which will build the chip and have rights to use and market it.

The third contender is Cyclotomics Inc. of Berkeley, Calif., a company that has done extensive work for the military in satellite communications systems. Cyclotomics was founded by a mathematician from the University of California at Berkeley, Elwyn R. Berkekamp, who devised the first decoding algorithm for Reed-Solomon codes in the 1960s.

Cyclotomics has placed some 600 discrete versions of its error-correction system in 12-in. read-only drives. It says that it, too, expects to have ICs in 90 days.

LOST IN SCRAMBLE. An ad hoc committee of the American National Standards Institute is currently trying to develop a number of standards for optical drives. Under study are such basic concerns as rotational speeds as well as more complex matters, such as error correction. But Cyclotomics marketing director Joseph K. Post expects the standards issue to be buried in the battle to establish a market.

"There are huge resources in the U. S. and Japan working at breakneck speed to place write-once and erasable 5¼-in. optical drives on the market," says Post. "As of this moment it is fair to say that each one is proceeding with its own error-detection-and-cor-



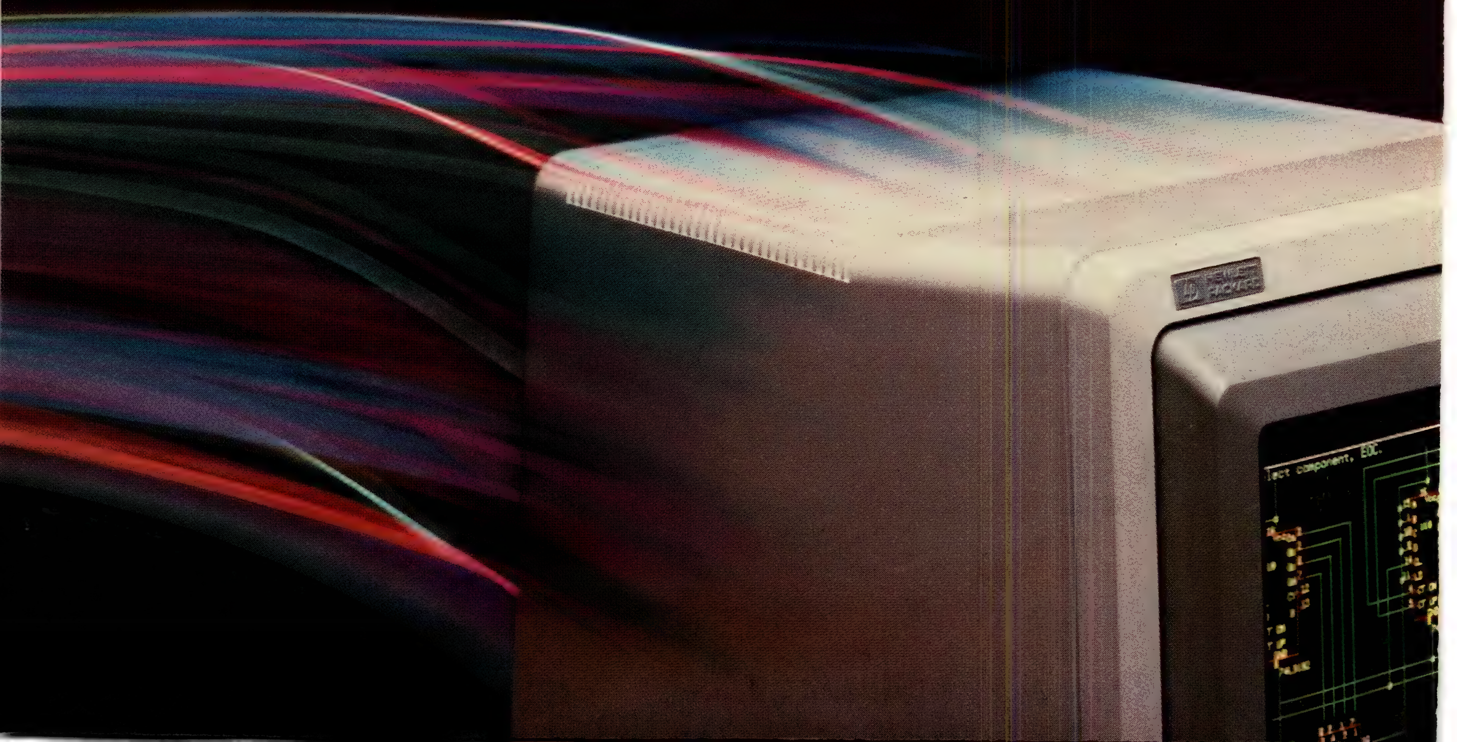
ARCHIVE. Optotech's optical drive, like others, needs a powerful error-correction scheme to lower error rates.

Name the computer that's so modular and expandable it lets you upgrade from 16-bit to 32-bit processing...

Expand from .5 to 7 Mbytes of memory...

Or go from monochrome display to high-resolution color graphics...

All in a snap...



loves changes

In addition, there are a number of HP peripherals for you to choose from: input and mass storage devices, plotters, printers, and more.

Productive programming language options.
You also have a complete set of programming language tools to work with, to help you better meet the needs of your application. For instance, the Series 300 runs HP BASIC, as well as HP-UX — HP's robust version of AT&T's System V UNIX™ operating system. And HP-UX supports industry standard programming languages, too — FORTRAN 77, Pascal, and C.

Link entire systems, not just users.
The Series 300 is designed to be linked with other systems. Your initial application may call for a simple, single-user system. But the Series 300 has what it takes to grow into a sophisticated 100-node LAN based on IEEE 802.3 or Ethernet™. With LAN, the Series 300 can share data with the Series 200 and 500 computers in the HP 9000 family, plus the popular HP 1000 and 3000 family.

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ELECTRONICS WEEK

MIT BUILDS TINIEST TRANSISTOR

Massachusetts Institute of Technology researchers have fabricated what is believed to be the world's smallest silicon transistor. The MOS FET device has a channel length of 600 Å, which is 1/17 the length of those of the smallest commercial transistors. MIT says cooling the device to cryogenic temperatures shortens electron transit times (called velocity overshoot), improving high-frequency response. Future work will aim at reducing impurities so that the transistor will run faster at higher temperatures.

IBM REORGANIZES U. S. SALES FORCE

To eliminate any overlap in its sales and marketing work, IBM Corp. last week reorganized its National Accounts and National Marketing divisions to form two geographic entities. The two new groups, the North-Central Marketing Division and the South-West Marketing Division, will market all products to customers in their areas. National Accounts sold big-ticket items to Fortune 1,000 companies and National Marketing handled smaller customers. IBM also merged a number of the marketing activities of its National Distribution Division. The changes are effective Jan. 1.

GD BUYS VLSI DESIGN EXPERTISE

Silicon Compilers Inc. will lend its very large-scale-integration design expertise to General Dynamics Corp. Under a $1 million three-year technical-assistance agreement, the company will assist in applying silicon compilation to VLSI designs for GD's military and aerospace programs. In exchange, the defense contractor will tutor Silicon Compilers in military chip-design requirements. GD also bought a 5% interest in Silicon Compilers.

PYRAMID LURES DATAQUEST HEAD

Pyramid Technology Corp. made David Crockett an offer he couldn't refuse: the presidency and an equity position in the superminicomputer maker. Crockett, former chief executive officer of Dataquest Inc., will be replaced at the market-research firm by Manny Fernandez, senior vice president and general manager, who joined a year ago after leaving his post as founder and president of Gavilan Computer Corp. Crockett says he turned down earlier offers to join Pyramid, but changed his mind after seeing the computer maker's latest financial statements. Pyramid's sales tripled to $35 million this year.

CREDIT CARDS GET SMART

Mastercard International, Inc. last week issued its long-awaited integrated-circuit credit cards [*Electronics-Week*, June 3, 1985, p. 44] to 40,000 customers. The "smart cards" were issued as part of a pilot program being conducted in Columbia, Md., and Palm Beach, Fla. Nationwide use could come as early as 1987.

BONN THROWS IN WITH EUREKA

While the West German government remains cool toward the U. S. Strategic Defense Initiative, it is shaping up as a major supporter of the French-proposed Eureka. The nondefense program aims to push European technology to U. S. and Japanese levels [*Electronics*, July 22, 1985, p. 30]. West Germany's Ministry for Research and Technology has approved funds of nearly $360 million for 1987-90 that companies can draw upon for Eureka projects. About $20 million has been set aside in the ministry's 1986 budget for Eureka-related studies.

NOW APPLE SUES JOBS

Apple Computer Inc. is suing former chairman Steven P. Jobs for founding a new educational computer company while still on the job. It also seeks to prohibit Jobs from using any confidential company information and from hiring away other employees. Also named in the suit is Richard A. Page, who Apple says had primary responsibility for designing its next computer, possibly the Motorola 68020-based Macintosh upgrade dubbed Jonathan.

JAPAN CHIP FIRMS CUT SPENDING

Four of Japan's major chip makers, all based in Tokyo, have announced deep cuts in capital spending. Toshiba Corp., which trimmed its estimates in July, followed that with another cut last week, down to $416 million from its original goal of $500 million. Other capital spending cuts include NEC Corp., down to $500 million from $583 million; Hitachi Ltd., down to $375 million from $542 million; and Fujitsu Ltd., down to $250 million from $417 million. Most of the cuts represent reductions in plant construction. Research and development allotments, companies say, are remaining at budgeted levels.

95 NEW ESPRIT AWARDS MADE

The European Communities last week nearly doubled its electronics research projects by announcing 95 new Esprit (European Strategic Program for Research and Development in Information Technology) project awards. Nearly 75% of the projects that received research funds last year are now operating productively and successfully, the EC claims. All told, Esprit now has more than 170 active projects. Esprit awards are made for projects in microelectronics, software, and information processing.

APOLLO SEES LOSS, CUTS STAFF BY 300

Apollo Computer Inc., which grew into a $250 million company in five years, will report a loss for the quarter ending in September. In response, the Chelmsford, Mass., maker of engineering work stations will slash some 300 jobs, which together with attrition reduces its work force by 12% to 3,400 worldwide. The company blames declining original-equipment-manufacturer business for its problems. On the other hand, Apollo reports a 50% increase in its sales to end users.

EXPERT FINANCIAL SYSTEM READY

Applied Expert Systems Inc. announced what it claims is the first commercial financial-services product that uses expert-system technology. The Cambridge, Mass., company's turnkey system, called PlanPower, consists of a 6,000-rule financial-planning knowledge base and the recently announced Xerox Corp. 1186 artificial-intelligence work station. It sells for under $50,000.

NTT CLAIMS FASTEST ARRAY

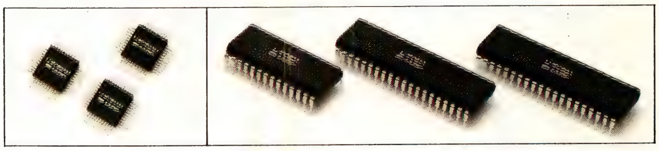
Nippon Telegraph & Telephone Corp. claims it has developed the world's fastest gate array. Per-gate signal-processing time of 165 ps compares with 267 ps for the fastest existing gate array. The new 5,000-gate device, measuring about 1 cm^2, uses NTT's Super Self-Aligned Technology, and U-groove isolation to separate each gate. It is designed for large general-purpose computers and supercomputers.

SHARP was first in the world to make a 4-bit 1-chip microcomputer with CMOS process. Now SHARP adds the 8-bit Z8 and Z80 series in CMOS.
Concept of our development — "Low Power Consumption, High Reliability and High Level of Integration". Using advanced CMOS process, SHARP brings technology solutions to customer's problems. The Z8 and Z80 CMOS series are completely pin-compatible with the conventional NMOS family. And, the quad-flat package (QFP) greatly facilitates surface mount assembly. Check out the countless applications at every turn: office automation equipment, telecommunications, control equipment, etc. SHARP accelerates the drive toward an energy-saving, high-performance microcomputer system.

Z80 CMOS

Z80 CMOS is the optimum device for a system where the lowest power consumption is required. Applicable for battery driven equipment.

- Available in standard or special "L-type" with ultra-low power consumption. In L-type, the standby mode requires only a few microamperes.
- Both 2.5MHz and 4.0MHz are available.



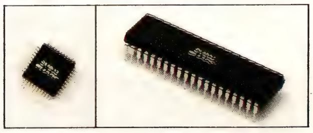
Z80 CMOS Family (8-Bit CMOS Microcomputers)

Type No.	Description	Features	Package
LH5080 LH5080M LH5080A LH5080AM	Central processing unit	● 8-bit microprocessor compatible with LH0080 (Z80 CPU) of NMOS process. ● Fully static operation. ● 10mA (TYP.) supply current. ● 2.5MHz (MAX.) clock frequency. (LH5080, LH5080M) ● 4.0MHz (MAX.) clock frequency. (LH5080A, LH5080AM)	40 DIP 44 QFP
LH5080L LH5080LM LH5080AL LH5080ALM		● Equivalent to LH5080. ● Power-save mode with the execution of HALT instruction. ● 50μA (TYP.) in power-save mode.	
LH5081 LH5081M LH5081A LH5081AM	Parallel I/O controller	● Compatible with LH0081 (Z80 PIO) of NMOS process. ● Fully static operation. ● 2mA (TYP.) supply current.	40 DIP 44 QFP
LH5081L LH5081LM LH5081AL LH5081ALM		● Equivalent to LH5081. ● Power-save mode with the execution of HALT instruction. ● 50μA (TYP.) in power-save mode.	
LH5082 LH5082M LH5082A LH5082AM	Counter timer circuit	● Counter/timer device which is compatible with LH0082 (Z80 CTC) of NMOS process. ● Fully static operation. ● 2.5mA (TYP.) supply current.	28 DIP 44 QFP
LH5082L LH5082LM LH5082AL LH5082ALM		● Equivalent to LH5082. ● Power-save mode with the execution of HALT instruction. ● 50μA (TYP.) in power-save mode.	

Z8 CMOS

Z8 CMOS makes control equipment more compact and cost-effective.

- Power savings with two types of standby modes: "stop"/"hold".
- Operates from DC-8MHz.



Z8 CMOS Family (8-Bit CMOS 1-Chip Microcomputers)

Type No.	Cycle time MIN. (μS)	Supply voltage (V)	Current consumption TYP. (mA)	No. of inputs/outputs	ROM (bit)	RAM (bit)	Subroutine nesting level	Package	Remarks
SM803	2.2	5	2.4	32	4096x8	144x8	Uses RAM area	40DIP 44QFP	Z8 CMOS type (pin compatible to NMOS Z8)
LU800V1	2.2	5	12	32	—	128x8	Uses RAM area	40DIP 44QFP	For development of SM803 For pilot production

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column decoding architectures, which enable data to be strobed from one column of cells in CMOS chips, are offering access speeds of 30 to 25 ns. Many have stretched memory arrays into elongated shapes to squeeze dice into 300-mil-wide dual-in-line packages, once again a de facto industry standard.

VARIETY OF DESIGNS. At the dawn of the megabit era, DRAM makers have a wider range of potential customers than ever before. As a result, up to 20 variations of 1-Mb chips are on the drawing boards. Some niches—such as video RAMs with on-chip multiple serial ports—promise to be large markets in themselves, and several producers are planning to avoid the mainstream price competition by introducing by-4- and by-8-bit widths before by-1s.

Most die layouts have been designed to support by-4-bit word widths. But the majority of producers are still planning to start megabit portfolios by introducing more conventional by-1-bit configurations, which are preferred in large computer systems. Some plan to follow the by-1-bit chips with 256-K-by-4-bit introductions within weeks.

Survival may hinge on knowing which versions to introduce first, says William C. Woodruff, strategic marketing manager for memory products at Mostek Corp. The Carrollton, Texas, company—which in the late 1970s was the world's leading shipper of DRAMs—hopes to make a comeback with the introduction of a by-4-bit megabit chip early next year. However, Mostek still has not begun volume deliveries of its delayed 256-K-by-1-bit and 32-K-by-8-bit chips.

The United Technologies Corp. subsidiary has working silicon on the 256-K-by-4 MK44E6 1-Mb chip and the 128-K-by-8-bit MK48E6 is also in the works. Both are made from 1.2-μm CMOS, using a double level metal double-polysilicon structure that Mostek developed for the delayed n-MOS 256-K models. "The 256-K being as late as it has been can be attributed to the learning curve on double-level metal. But we feel we have suffered that delay and have learned well from it," says Woodruff.

Mostek also attempted to introduce the world's first by-8-bit DRAM when it introduced the 32-K-by-8-bit MK4856 in 1983. Today, it is planning its entry with the by-4-bit megabit chip because "the volume acceptance of a 256-K-by-4-bit will occur sooner than the volume acceptance of a by-8," Woodruff states. "The acceptance on the by-1 megabit will be the fastest. However, that is where all the competition is, and I anticipate a rather aggressive pricing environment."

Putting a million bits on a chip looks to be a big technical barrier

As with earlier DRAM development, the success of megabit product development depends on a familiar but frustrating tradeoff—the use of new circuit designs and processing techniques for smaller dice versus more mature technologies that usually yield larger but more manufacturable chips. "That's what fortunes and careers are made on," says Lionel White, program manager for 1-Mb DRAMs at TI in Houston.

TO TRENCH OR NOT. Other pivotal technical decisions are being made; among them is whether to use new trench memory-cell capacitors, which are carved down into the silicon substrate to reduce the planar surface necessary for plates large enough to hold a stable charge. Reliable trench capacitors are considered difficult to make, but several companies are tackling the hurdles, believing the long-term payoff will be smaller, low-cost, faster memories. These companies also hope to spin off the trenching technique into other logic and memory MOS products.

"Initially, trench capacitors scared us, too," says White. "It was, however, something that we felt would have an evolutionary path to the 4-Mb level. So we decided to go ahead and take the risk, putting heavy development resources into trenches. We now have a pretty good process and capacitors." TI began distributing engineering samples of its 1-Mb-by-1-bit chip in August. MOS-memory officials in Houston have targeted general sampling for early 1986.

The difficulty with trenches is controlling the profile of the etched groove, says White. "The beauty of trenches is that if you need more capacitance, you go deeper [for more active area]. The tradeoff is between soft-error rates

MEGABIT SCORECARD: THE PLAYERS AND THE TECHNOLOGY

Players	Status and goal	Organization	Technology	Die size (mil²)	Capacitor (type, fF)	Package
Advanced Micro Devices	Final design, samples by second or third quarter	By-4, by-1	CMOS 1.2 μm, double metal	70,000	Trench, NA	300-mil DIP, surface mounted
AT&T	Sampling, volume by year end	By-4, by-1	CMOS 1.3–1 μm, single metal	69,000	Planar, 40	300-mil DIP, surface mounted
Fujitsu	Engineering samples	By-1	n-MOS 1.8 μm (stacked cell); single	84,000	Planar, 55	NA
Hitachi	Engineering samples	By-1	n-MOS 1.3 μm, double	73,000	Planar, 70	NA
IBM	In production	By-4, by-2 by-1	SAMOS NA n-MOS 1 μm, single	SAMOS: 90,000 n-MOS: 75,000	SAMOS: Planar, 43 n-MOS: Planar, 37	480-mil 23-pin grid array 300-mil DIP
Intel	First silicon	By-4	CMOS 1 μm, single	82,000	Planar, 48	NA
Micron Technology	Silicon by year end, samples first half	By-1 in n-MOS; 20 variations	n-MOS 1.5 μm, single CMOS 1.5 μm, single	110,000	Planar, 65	n-MOS: 300-mil, 18-pin, ceramic CMOS: Plastic Zigzag In-Line Package
Mitsubishi	Engineering samples, samples by spring	By-1	n-MOS 1.2 μm, single	100,000	Planar, 45	300-mil 18-pin DIP
Mostek	Working parts, samples early 1986	By-8, by-4	CMOS 1.2 μm, double	106,000	Planar, 33	300-mil 20-pin DIP, surface mounted
Motorola	Final design, samples by first quarter	By-1	CMOS 1.2 μm, double	80,000	Planar, 50	300-mil small-outline J-lead DIP, surface mounted
NEC	NA	By-4, by-1	n-MOS 1.5 μm, single	67,000	Trench, 60	16-pin
Texas Instruments	Engineering samples, samples by first qtr.	By-4, by-1	n-MOS 1.5 μm, single	80,400	Trench, 50	300-mil SOJ DIP
Toshiba (Siemens, second source)	Working parts, samples by October	n-MOS by-1 CMOS by-4, by-1	n-MOS 1.2 μm, double CMOS 1.2 μm, double	98,000 97,000	Planar, 42	300-mil 18-pin DIP
Vitelic	Final design, samples by first half	By-4, by-1	CMOS 1.2 μm, single	80,000	Flat, 35	300-mil DIP

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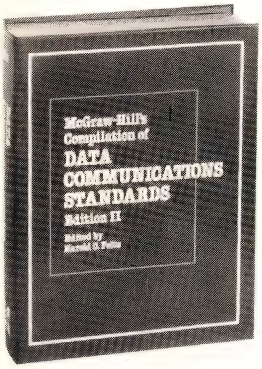

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Telecom Australia will fund a broad range of programs over the next year. These will include the start of an optical-fiber trunk network linking state capitals, installation work for a cellular radio system, and progress on an integrated digital network to provide enhanced business services. Also expected are new products such as cordless telephones and electronic messaging services, as well as the introduction of satellite business services.

Telecom will have 52 technical papers at Ireecon, many of them covering optical fiber projects and the integrated services digital network. Ireecon 85 delegates will hear about the Sydney-to-Melbourne optical-fiber trunk route, which will span 1,000 km and use primarily single-mode fibers. The link will provide eight 140-Mb/s and six 565-Mb/s carriers. Deliveries of transmission equipment and cable will begin next year, with the $35 million project set for completion by early 1988.

The plan is to link with optical fiber by 1990 all capital cities, including Adelaide and Darwin, which are separated by 3,000 km of virtual desert. To make cable installation in remote regions of Australia more economical, Telecom Australia's research labs are investigating fiber optics. One paper by Telecom engineers outlines current research into new glass materials to achieve lower transmission losses.

Strengths lie in university R&D and telecom

These ambitious plans to wire the country with optical fiber have spawned a large fiber-manufacturing industry over the past year. Two major consortiums have emerged—one using technology from Corning Glass Works of Corning, N. Y., the other linked with Sumitomo Corp. of Osaka, Japan.

MICROWAVE OUTLOOK. Besides conductor-based networks, Australia relies heavily on microwave links for its long-haul broadband communications. A paper from the Microwave Technology Development Centre of the University of Queensland argues that microwave is a key technology for Australia and has substantial export potential.

The microwave center has found commercial application for its research through an association with Adelaide-based Codan Pty. Codan has incorporated radio-frequency microwave electronics developed by the center into outdoor satellite-receiving dishes being developed for the Australian satellite network, Aussat. A Codan-led consortium is also tapping the center's expertise to develop small Ku-band earth stations to be used with Intelsat satellites.

The Australian satellite program, with its new antenna design, will be outlined in 17 papers at Ireecon. The chief designer of the system, Wayne Nowland, will explain its features in one of the papers. The satellites incorporate 12- and 30-W transponders and the antennas can synthesize 10 communication beams.

Ireecon has never been seen as a venue for computers and information-processing equipment, so these products will be only a minor part of the show, even though Australia has a relatively large market for computers. Nearly every major world computer company has a local presence Down Under.

LOW PRODUCTION. Australian-owned computer manufacturers, a large number of small companies, produce only about $35 million worth of products annually, a fraction of the total market, which for 1985 is estimated at $1.5 billion (see table). They are hampered by the refusal of government purchasers to specify local product and the fact that most key components have to be imported. Prospects for the software industry are more promising, with annual sales estimated at $210 million.

The show is popular with instrument distributors and makers, though again most of the product on display will be imported. There is only one major Australian-owned instrument maker, BWD Instruments Pty. of Melbourne, which will exhibit its range of oscilloscopes.

During the early days of the IREE in Australia, the organization garnered many members from the radio-broadcast industry, so Ireecon traditionally has a strong broadcast and TV section. More than 40 exhibitors will display broadcast-related wares, from locally made antennas and audio equipment to imported high-ticket gear for digital studios. Much of the high-end broadcast equipment at Ireecon will be new for Australian audiences, but has already appeared at June's Montreux International TV Symposium in Switzerland and last spring's National Association of Broadcasters convention at Las Vegas.

Competing for attention with the eye-catching stands of broadcast companies will be the component distributors. Australia imports virtually all of its semiconductors ($105 million this year) and much of its componentry. Although companies must import most components, there are pockets of manufacturing activity in switches, capacitors, hybrids, and medium-scale-integration custom chips. However, the lifting of tariff protection in the mid-1970s resulted in the collapse of the industry as cheaper imported goods flooded in. ☐

Craig Addison is editor of Australian Electronics Engineering *magazine.*

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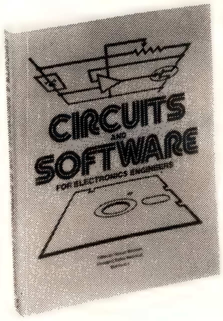

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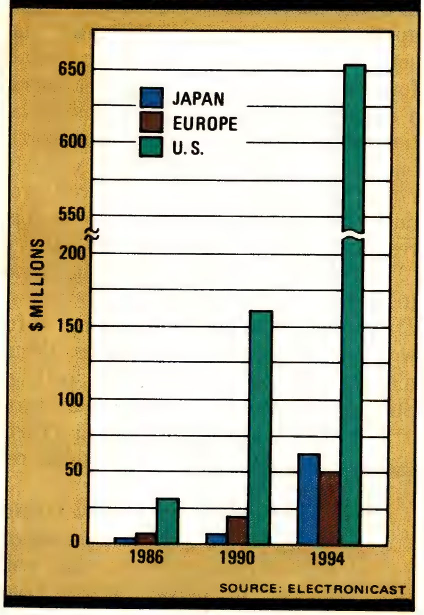
gram) has the widest support because it has the advantage of simplicity over the integrated optics unit, which gathers optical components on a hybrid input/output chip. More than 20 companies worldwide already have plunged into work on fiber-optic gyroscopes, according to Electronicast estimates.

U. S. TO REMAIN THE LARGEST MARKET



SOURCE: ELECTRONICAST

The first commercial all-fiber gyroscope, due on the market soon, has been built by SEL AG in Stuttgart, West Germany. As a rate gyro, it has a drift rate of about 12°/hour, no better than today's conventional units. Its designers point out, however, that it is an early version. Thomson-CSF in Corbeville, France, has done even better with a laboratory prototype, attaining a drift rate of 0.3°/hour for a gyroscope that has a volume of only 0.1 liter [*Electronics*, Aug. 5, 1985, p. 20]. In the U. S., McDonnell Douglas Astronautics Co., Huntington Beach, Calif., is nearing the product stage with its all-fiber-optic gyro.

GYRO WORKERS. Both Moore and De Paula's main interest also centers on the rotational sector of sensing. Moore's Litton division is a major manufacturer of military and commercial guidance equipment, where gyroscope improvements are of central importance. And De Paula is developing guidance hardware for a new generation of spacecraft for which the Jet Propulsion Laboratory is responsible.

The most critical task before developers of fiber-optic sensors now is to develop the glass components that are in short supply, including laser diodes, polarizers, modulators, couplers, and the integrated optics to tie them together efficiently. Some companies are starting designs, but how fast they materialize "all depends on funding and market need," says Moore. ☐

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ness where one guy wins. There is a natural inclination to standardize, and if you lose, you lose big.”

Microsoft has won big so far with MS/DOS and Xenix, where it has leveraged its ties both to IBM and to Intel Corp.’s microprocessor architecture. But the jury is still out on Windows.

CLOSING THE WINDOW. “Having a separate applications package running in Windows is better than having integrated software, because you can use a real ‘power’ application with other software,” says analyst Murphy. “In effect, you integrate your own package.” But he notes that Windows and Topview are mutually exclusive for applications writers, and Microsoft will have to attract enough of them for its package to succeed. Ballmer agrees: “It may take three years to shake out until the major ISV’s [independent software vendors] move to the next application cycle.”

Besides developing new products, Microsoft, under Shirley, has reorganized its product-distribution procedures. “We were late in recognizing the importance of selling to national accounts,” Shirley says. “Then we tried to switch our sales people, who called on dealers, to national accounts, and it didn’t work. Now we’re hiring professionals and it’s working well.” Microsoft still uses dealers, but to sell applications software to large accounts, he says, “you’ve got to be there in person.”

HITTING THEIR STRIDE. At 48, president Jon Shirley (left) is Microsoft’s elder statesman. Chairman William H. Gates is 30.

Noting that chains of retailers were beginning to squeeze out independent retailers, Shirley has cut the number of distributors from 30 to 5 because “you don’t need distributors to sell to chains.” Moreover, Shirley says, distributors tend to compete by cutting prices, a factor that cuts Microsoft’s share of sales.

More than 30% of Microsoft’s business is international, and what Shirley calls a “very healthy” part of it is in Japan, where Microsoft’s MSX graphics software has been adopted for home computers [*Electronics*, July 1, 1985, p. 19]. However, Shirley says candidly that low-cost graphics computers from Atari Inc. and Commodore International Ltd. “will shut Japan and MSX out of the U. S. market.”

Microsoft has discussed doing development work with both of these companies, but decided not to. “Our resources are already committed,” Shirley says. “It would be a major effort on our part. You can’t take a Macintosh program and revise it in 30 days.”

As Shirley, Cole, and Ballmer direct day-to-day operations, Gates remains the strategic leader. His goal: a microcomputer in every home, a microcomputer on every office desk. “Eventually the price of a desktop work station won’t be much greater than the desk it sits on,” Gates says. “And we’ll provide the software.”

Gates says that Microsoft is in a strong position. “We have a balanced approach, not tied to any individual product or contract. At no time has IBM accounted for more than 10% of our sales. Our main assets are our methodology, our software tools, and our reputation.”

Another strength, Shirley says, is the company’s handling of its technical work force. “Any individual product has a program manager to work on development and a product manager to interface with the outside world. We don’t force into management [positions] people who don’t want to do that kind of work and whose time is better spent elsewhere.” Gates claims this structure makes Microsoft the most stable of any microcomputer software company. “You won’t see any changes [in this strategy] in the near future.”

Microsoft’s strong growth has brought up the temptation to take the company public and provide an opportunity for employees with stock options to cash in on their success. There are no specific plans to go public, but the issue will be seriously considered next year, Gates says.

The danger in such a move is that he might lose control of Microsoft much the way Steven Jobs did at Apple Computer Inc. [*Electronics*, Sept. 23, 1985, p. 19]. This possibility doesn’t appear to faze the affable Gates. “If the people who run the company don’t like what you do, maybe you should lose control.” But he doesn’t appear worried by the prospect.

–Clifford Barney

BOTTOM LINES

TECHNICAL MANAGERS STILL HARD TO FIND . . .

A new survey confirms what many electronics executives have felt: it was harder to find key people with high-tech engineering, marketing, and managerial skills in 1984 than in 1983, and this difficulty has continued into 1985. Thomas-Mangum Co., a Los Angeles management consultant, said that of those who responded to its sixth annual Survey of Executive and Professional Manpower Markets, 46% said they had difficulty attracting key personnel, up 6% from 1983. Further, 64% of the respondents said they expected no change in 1985.

. . . AND SCARCITY SLOWS PROGRESS

Another survey—from PA Technology, management consultants in Princeton, N. J.—concluded that a shortage of qualified staff is the main constraint on the development of new products and processes in the major industrial nations. Of those executives surveyed in the U. S., Japan, West Germany, Britain, and Belgium, 22% cited manpower shortage; none thought the high interest rates or unions were barriers to innovation. These traditional scapegoats “have been overshadowed by a very real fear that we are simply not producing enough qualified people,” said Peter Hyde, president of PA Technology.

LISP MACHINE ADDS TO FINANCING

Lisp Machine Inc., the Cambridge, Mass., developer of machines for use in artificial intelligence, has added to its coffers again. The company recently got a $4.5 million infusion from Raytheon Co., Lexington, Mass. [*Electronics*, Sept. 9, 1985, p. 83]. Now it has raised another $6.1 million in venture capital, bringing its total financing to $18.1 million. A major participant in the latest financing was General Signal Corp. The Stamford, Conn., conglomerate invested $5 million to tap Lisp’s AI expertise, which “will become increasingly integrated into General Signal’s electronic, energy, and process systems businesses,” a spokesman said.

CALAY SYSTEMS GETS NEW FUNDING

Calay Systems Inc. has received $7 million in new venture financing. The three-year-old Irvine, Calif., maker of computer-aided design systems said it will use the funds for ongoing research and development work.

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face, designated U, to the network-termination point at the customer's premises. The U is converted by the network termination point to the four-wire ISDN S and T interfaces, which link to the customer's telephones and terminals.

S and T have been set at a transmission rate of double the B and D channels, designated as 2B+D. Primary access (Fig. 1b) from the central office to a PBX in North America is set at a 23B+D format, which amounts to 1.544 Mb/s. Europe will stick to its 30B+D format, a rate of 2.048 Mb/s.

The big question before semiconductor market-planning groups is whether the S/T or the U interface will be the point of departure for wide-scale implementation of ISDN. The U interface is still undefined and thus is the sticking point in current international negotiations. "S and T were easy to define because there was never an international standard before. But U is going to be much harder to agree on because central-office standards differ so much between countries," says Bob Broomfield, an assistant vice president in the Semiconductor Division of Mitel Corp., Kanata, Ont., Canada.

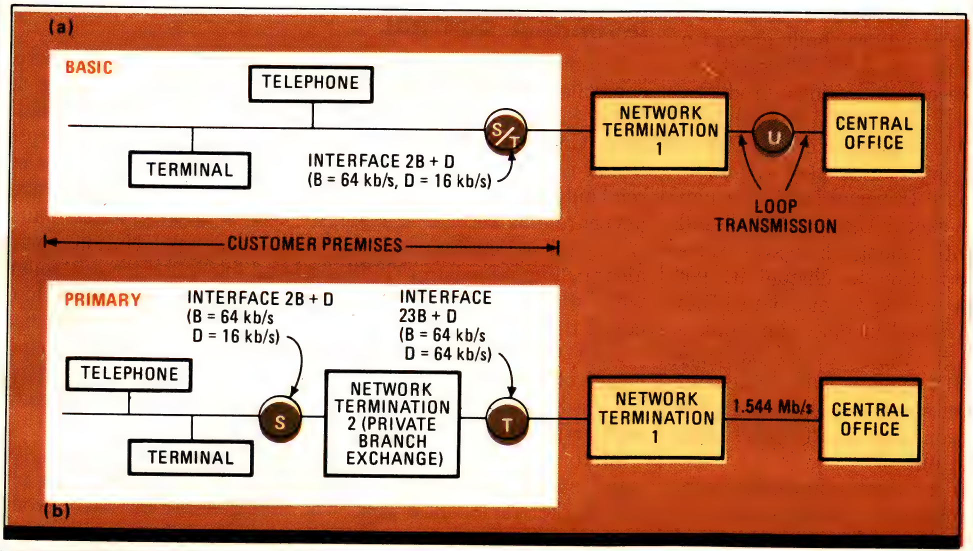
RAT'S NEST

Another position is that the S could become a rat's nest of proprietary implementations that will ultimately slow ISDN development. PBX vendors are more likely to forgo standards in favor of low-cost proprietary versions of the S interface, according to Motorola Inc. telecom-chip officials. The ISDN standard will likely get its biggest boost when software and services are made available through the phone companies and the U interface, says a Motorola representative. Only after the U is settled will the S interface have the applications base needed to keep costs in line, the company believes.

The U interface must increase the available bandwidth on the local loop, but the differences in loop installations among countries have created serious questions about the economic benefits of implementing it. Up to now, agreement has been reached favoring echo-cancelation schemes over time-compression multiplexing transmission. Now the burning question is which line-code method should be implemented. Vying for acceptance are differential biphase, alternate-mark inversion, and several block-coding schemes.

The Europeans tend to favor the block-coding schemes. In North America, AT&T Co. and Northern Telecom Inc. are backing AMI, and Mitel is among those pushing differential biphase as a cost-effective coding solution. The wild card in standards deliberations is Japan, which is pursuing its own version of ISDN.

1. NETWORK DEFINITION. Local-loop integrated services digital network transmission at the U interface (a) is still undefined, but inside the customer premises the S and T interfaces (b) are complete.



"In the standards-setting organizations we participate in, I've come across the positions of Siemens from Germany, Ericsson from Sweden, AT&T in the U. S., and all the rest, but the Japanese are a mystery," notes George Smyth, vice president of digital switching systems at Northern Telecom's Bell Northern Research Laboratories, Ottawa, Ont.

Japan's Information Network System is similar to ISDN but differs from European and North American systems by providing a three-channel customer interface of 64, 16, and 8 kb/s. The 64-kb/s channel carries digital telephone signals or high-speed data, including facsimile and videotex. The 16-kb/s channel carries low- and medium-speed data, including facsimile, videotex, telewriting, and teletex. The 8-kb/s channel is intended for network-customer signaling.

These channel definitions are not compatible with CCITT standards, but Nippon Telegraph & Telephone Corp., Tokyo, says it expects to convert the three-channel scheme to conform to CCITT standards in about three to four years—about the same time the CCITT should issue its recommendations. The primary rate is the same as in the U. S.—1.544 Mb/s. Service at half that speed is also available.

Although NTT expects to change the customer-interface channel capacity to match CCITT standards once they are set, it does not know if it will change from the time-compression multiplexing method it now uses to the echo-canceling approach favored by the U. S. and Europe. The time-compression multiplexing method is often called the ping-pong method because the two transmitters transmit one at a time in rapidly alternating succession.

"Use of the same interface capacity will provide international compatibility, regardless of the method of transmission to the customer," says Nobuo Inoue, manager of the Information Network System model at NTT.

HOME EQUIPMENT

The customer-premises equipment in the Japanese system includes a digital telephone and a digital service unit. The digital service unit has an 88-kb/s interface on the subscriber-line side that operates in a ping-pong mode. It has two customer ports, each with two channels for data and signaling. The port for digital telephone or other high-speed terminals has a 64-kb/s channel for carrying data and a 4-kb/s channel for signaling. A port for a lower-speed terminal has a 16-kb/s data-carrying channel and a 4-kb/s signaling channel.

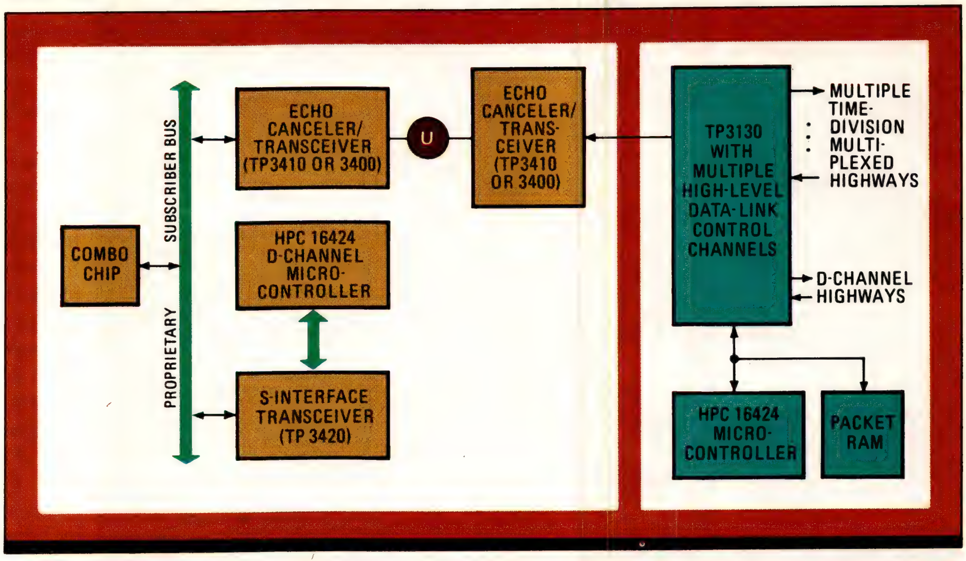
Large-scale ICs in the system are made by four companies—Hitachi, Fujitsu, NEC, and Oki Electric. The telephone itself houses three types of LSI chips: a codec, a telephone input/output controller, and a digital-service-unit interface controller. It also makes use of other standard and hybrid ICs. The digital service unit includes four LSI chips of three types—two 256-bit memory chips, one equalizing amplifier, and a digital interface chip.

The manufacturers will not talk about these chips, which in any event will be superseded when NTT changes its interface. They say that commercial chips are at least six months off, and are unwilling to say what they will offer in the future.

The Japanese decision to go their own way could be a wise one because incomplete standards are holding back the ISDN, according to financial an-

and data at 80 kb/s over 2 km. Motorola is now working on a second version that will boost the rate to 160 kb/s over 2 km when introduced early next year. Both versions use a two-wire interface, as opposed to ISDN's four-wire S interface.

Also next year, Motorola will introduce a version with ISDN signaling, but the enhanced chip will still use a two-wire interface and send data at 160 kb/s over 2 km. Late in 1986, Motorola expects to complete work on an S/T-interface chip that conforms to the ISDN's four-wire interface and sends data at 144 kb/s over 1 km. For 1987, Motorola has slated the completion of a four-wire ISDN U-interface chip that will handle 160 kb/s.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TP3130 WITH MULTIPLE HIGH-LEVEL DATA-LINK CONTROL CHANNELS
MULTIPLE TIME-DIVISION MULTI-PLEXED HIGHWAYS
D-CHANNEL HIGHWAYS
HPC 16424 MICRO-CONTROLLER
PACKET RAM

3. U TURN. National Semiconductor Corp. is going with a proprietary interface bus as part of an evolutionary strategy. The TP3400 transceiver/echo canceler handles private-branch-exchange short-loop applications up to 6,000 ft and the TP3410 for loops of several miles.

"The UDLT chips today offer twice the distance with half the wires," claims Mike McCroskey, Motorola's product-planning manager for telecommunications in Austin. McCroskey says the reduction in wires and doubling of distances will translate into about half the cost to implement system-specific signaling schemes, compared to the emerging S interface of ISDN. Motorola telecom-chip executives believe that the cost reduction will be too much for equipment manufacturers to resist. The result will likely be a combination of low-cost and high-performance proprietary digital lines plus ISDN-compatible links at the user sites.

HOUSEKEEPING FUNCTIONS

Intel Corp. is focusing on line-card and S-interface chips with the iATC family of components. Current offerings include the 29C50/51 programmable feature-control combination, the 2952 line-card controller, and the 29C55 two-wire digital transceiver. Scheduled to be introduced soon is the 29C53 four-wire S-type transceiver. These take care of the housekeeping functions needed to move either voice or data signals from the line card to the ISDN subscriber's equipment, according to Graham Alcott, telecommunications marketing manager at Intel's unit in Chandler, Ariz.

The iATC 29C50 and 29C51 are user-programmable codec and filter combinations designed for use in switching environments with synchronous transmit and receive channels. When combined with the 2952 on an analog line card, they provide all the pcm encoding and decoding, channel filtering, signal multiplexing, line-card addressing, signaling and feature-control functions for each analog line-interface circuit. All are fabricated using Intel's CHMOS process.

The 29C50/51 chips have three on-chip hybrid balance networks. These can interpolate between two external networks for two- to four-wire conversion. Three independent programmable gain amplifiers trim the transmit and receive voice-path signals and the hybrid error signal. A secondary analog output, which is digitized by the 29C50/51 independently of the analog voice signal, produces a second 8-bit companded pcm word. The 29C50/51 can decode a secondary analog output according to its digital output.

The 29C50 has 10 signaling channels. Three are for transmitting, three for receiving, and four are programmable for either transmitting or receiving. The 29C51 has seven signaling channels configured as one for transmitting, two for receiving, and four programmable channels. The channels are programmable for either European or U.S. standards for voice encoding, and the user can select a variety of testing modes to simplify centralized diagnostics.

The iATC 29C52 is designed to be used on analog line-interface cards equipped with the 29C50/51 feature-control combinations as well as with on-line cards serving digital subscriber lines equipped with digital line-interface circuits. It concentrates and multiplexes all digital information passing between the line card and the next switching or control level in a system hierarchy.

The Intel chip manages all transfers of data between the backplane and the 29C50/51 and facilitates connection with optional line-card microprocessors. It implements all protocol-control functions using the HDLC format for all data transmitted between the line card and the central switch. With eight serial, bidirectional ports for digital transmission of voice, data, control and signaling information to and from the subscriber, a single 2952 can control as many as eight 29C50/51s.

In addition to its primary role on the analog line-interface card, the 2952 is also designed for use in telemetry applications using multifrequency detection units, analog and digital trunk units, and special service units as well as the high-speed primary HDLC controller at the central control unit. It also has an interface that is compatible with single-chip CHMOS microcontrollers such as the 80C49 and 80C51 and with such direct-memory-access-compatible microprocessors as the 8088, 8086, or 80186. Through this port, the processor can access all information passing through the 2952, providing time-slot assignments and switch control.

TRANSCEIVER FAMILY

Intel is also introducing the first product in a transceiver family, the 29C55 communications interface and transceiver controller. The 29C55 allows extension of digital functions such as integrated voice and data directly into the subscriber equipment with a high-speed two-wire digitally encoded serial line. It is used with the 29C50/51, 2952, and a microprocessor for PBX applications. The 29C55 also includes a terminal-to-terminal mode that allows general data-communications functions. It incorporates transceiver and digital interface functions, which can be programmed for use at either end of the loop.

Capable of a 144-kb/s data-transfer rate, the 29C55 has four interfaces: a digital SLD 29CX telecommunications interface, a two-wire analog line interface, a general-purpose digital synchronous serial interface, and a general-purpose micro-

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Circle 51 on reader service card

develop appplications for the engine. Steve Swerling, vice president and general manager of Mentor's Computer Systems Division, says Mentor will soon offer the compiler technology for other languages, particularly Fortran.

A core feature of the compiler is its ability to take standard high-level-language source code, such as C code, and translate it into micro operations. The compiler is smart enough to analyze the source program to discover where parallel execution can be set up. It will recognize data dependencies, points at which an operation depends on data from a previous operation, so it will not schedule parallel execution of dependent statements and thereby invalidate an algorithm.

All Compute Engine machine instructions execute in one clock cycle. But each may contain several micro operations or primitives that can run in parallel. It is these operations the compiler combines to build single-cycle machine instructions, packing each instruction as full as possible—that is, scheduling as many primitive operations as possible for execution during each cycle. It is this feature more than any other that gives the accelerator its power.

SEMICUSTOM CIRCUITS

The Compute Engine processor architecture includes floating-point hardware, totally integrated into the CPU, that can deliver 8 million floating-point operations/s. The two-board engine, made from proprietary, semicustom-circuit technology, is capable of overall computation performance of up to 10 mips running the optimized compiled code. Mentor builds the processor circuits from 10,000-gate, 16-MHz, CMOS gate arrays from VLSI Logic Inc.

The company has done some initial testing using the C Whetstone benchmark—a version of the standard Fortran benchmarks using the C language and a mix of single-precision and double-precision floating-point calculations. The tests showed the accelerator can perform 2,750,000 C Whetstones/s. That performance is about seven times the speed of the DN660, Apollo Computer Inc.'s fastest work-station processor, which in turn is just a little faster than a Digital Equipment Corp. VAX-11/780 superminicomputer.

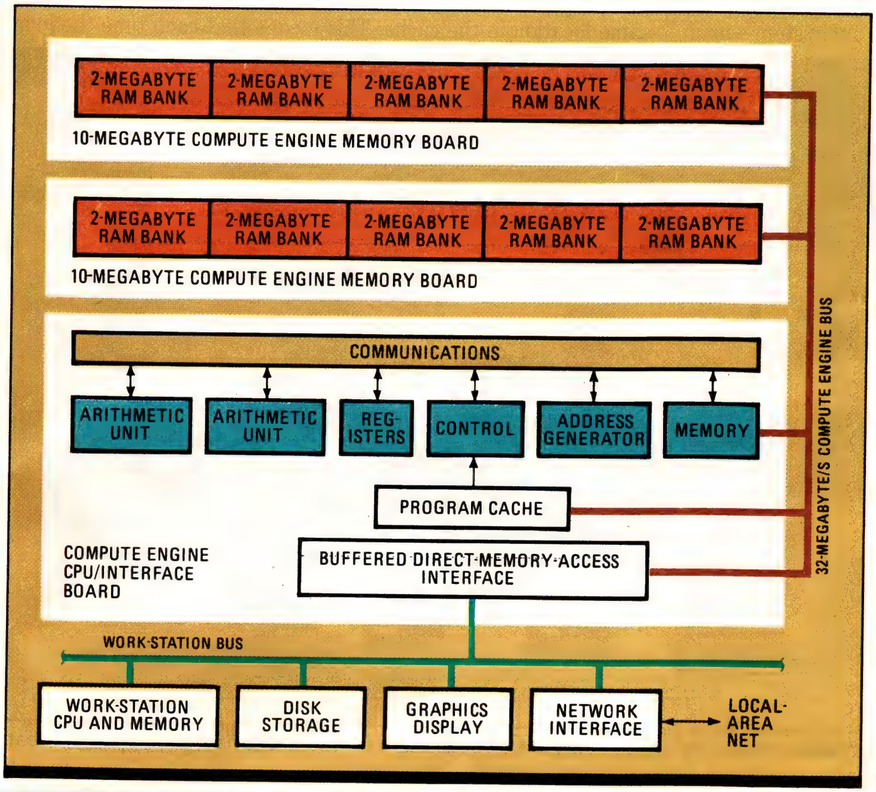
The Compute Engine has low-level parallelism using reduced-instruction-set-computer concepts. Low-level parallel architecture has one processor, but uses multiple, parallel functional units for arithmetic logic, register manipulation, address calculation, and the like (Fig. 2). This is in contrast to parallel machines that gain speed by connecting complete processors in parallel through a shared memory—high-level parallel architectures such as those from Sequent Computer Systems Inc. and Encore Computer Corp.

SOME RISC INVOLVED

The architecture uses three RISC concepts. First, machine instructions execute in one clock cycle. Second, only the primitive intructions are allowed in the instruction set. Third, the machine has a pair of large general-purpose register files—completely separate banks of registers. One has 1,024 address registers, which are used in conjunction with the address unit to improve subroutine linkages. The other has 872 data registers. Each multiprimitive machine instruction can contain primitives to read from two data registers and write to two other data registers. During the same instruction, it is also possible to do two reads out of the address registers and one write to them. This gives the compiler a lot of flexibility in building instructions.

The remaining major technology at work in the Computer Engine is its huge, directly addressable memory—up to 20 megabytes. Memory addressing is 32-bit, so up to four gigabytes of physical memory could be directly addressed, if necessary. Mentor could add storage in future versions when 1-Mb memory chips become available, or before that, when denser packaging is developed for the currently available 256-K chips. The company will consider the newer packaging technologies, such as surface mounting, when they have been proven sufficiently reliable. For now, it is using conventional packaging and printed-circuit technology.

2. PARALLEL PROCESSING. The central processing unit of the Compute Engine contains six computational units that operate in parallel. They are tied together by a communications unit.



The Mentor designers moved away from virtual memory in the Compute Engine because it does not have to do multitasking or multiuser computing in its intended application. It is geared to do compute- and memory-intensive jobs one at a time. Virtual memory would get in the way and add unneccessary overhead. The engineers also eliminated overhead associated with multiuser multitasking environments, such as state saving.

One type of overhead that is important—and difficult to eliminate—in a highly interactive application such as CAE is the overhead required for features such as a rich multitasking user interface, high-performance graphics, networking to other work stations, or a complex file system. Those functions are left up to the work-station part of the Mentor system.

The work stations, made by Apollo and based on Apollo's Domain architecture, are well suited to the purpose. The Compute Engine is well suited to running the compute-intensive applications programs. In fact, the two boards that make up the Compute Engine plug into the work stations' backplanes and connect to the work-station bus. The design results in a synergistic combination of functions—each structure doing what it does best to provide an overall job throughput of supercomputer proportions. □

is executed, the instruction is loaded into the cache and removed as soon as the data is fetched; the data, in turn, is kicked out when the instruction is fetched during the next iteration. This seesaw action continues as long as the loop is being executed, thus reducing the efficiency of the cache.

If the two items can reside in different places in the cache despite having the same low-order address bits, however, overall cache efficiency increases. This can be achieved by doubling the size of the cache to 8 K-bytes, splitting it into two 4-K-byte blocks, and alternating pieces of incoming information between these blocks. As a result, information designated by the same low-order bits can go to two places in the cache, a technique called two-way interleaving.

The penalty paid for two-way interleaving is that to maintain the speed advantages of cache, the cache lookup logic must be able to look in both places at once. Sequential operation compromises performance. Therefore, the lookup hardware must be doubled.

Four- and eight-way association caches are also possible, but the additional logic required is expensive. Making bigger caches is another way to improve cache performance. Because of the steep decline in prices of fast memory chips, a larger cache using two-way interleaving is an effective cost/performance tradeoff. And it is the alternative the Masscomp engineers chose.

BREAKING THE BUS BOTTLENECK

Another feature that helps match the speed of the memory subsystem to that of the new processor is the split-transaction bus protocol. Typically, a bus transaction has three components for reading information from memory: transmission to memory of the required data's main-memory address, access time to read data from memory, and delivery of the data. In bus schemes other than split-transaction, no other device can use the bus during any of the three phases, even though the bus is free of traffic during memory-access time. In the split-transaction bus protocol, typically found only in mainframe computers, one processor can issue a request to memory while the data requested by another processor is being read.

A memory subsystem using the split-transaction protocol must be smarter than simple memory systems. It has to keep track of which processor has made a request and deliver the correct data to the right processor. In the Masscomp design, this responsibility falls to a set of five additional bus wires with some associated logic, which keep track of memory requests until they are satisfied.

The memory is split in two blocks to support the split-transaction protocol. Each block has a first-in first-out buffer with four slots to hold the memory-access command, the identifier of the processor issuing the command, the address to be looked up in memory, and, if it is a write instruction, the data to be placed in memory.

A different type of bus also required a boost in its speed—the I/O buses used for transferring data to and from such devices as disk drives, tape drives, and network interfaces. The solution in the MC-5700 is a Multibus that operates at 2 to 3 megabytes per second for each processor. These Multibuses are not the standard 8- and 16-bit configurations, however. Rather, they are a superset of the IEEE-796 Multibus standard, allowing 32-bit I/O transfers when an optional block-mode adapter is installed.

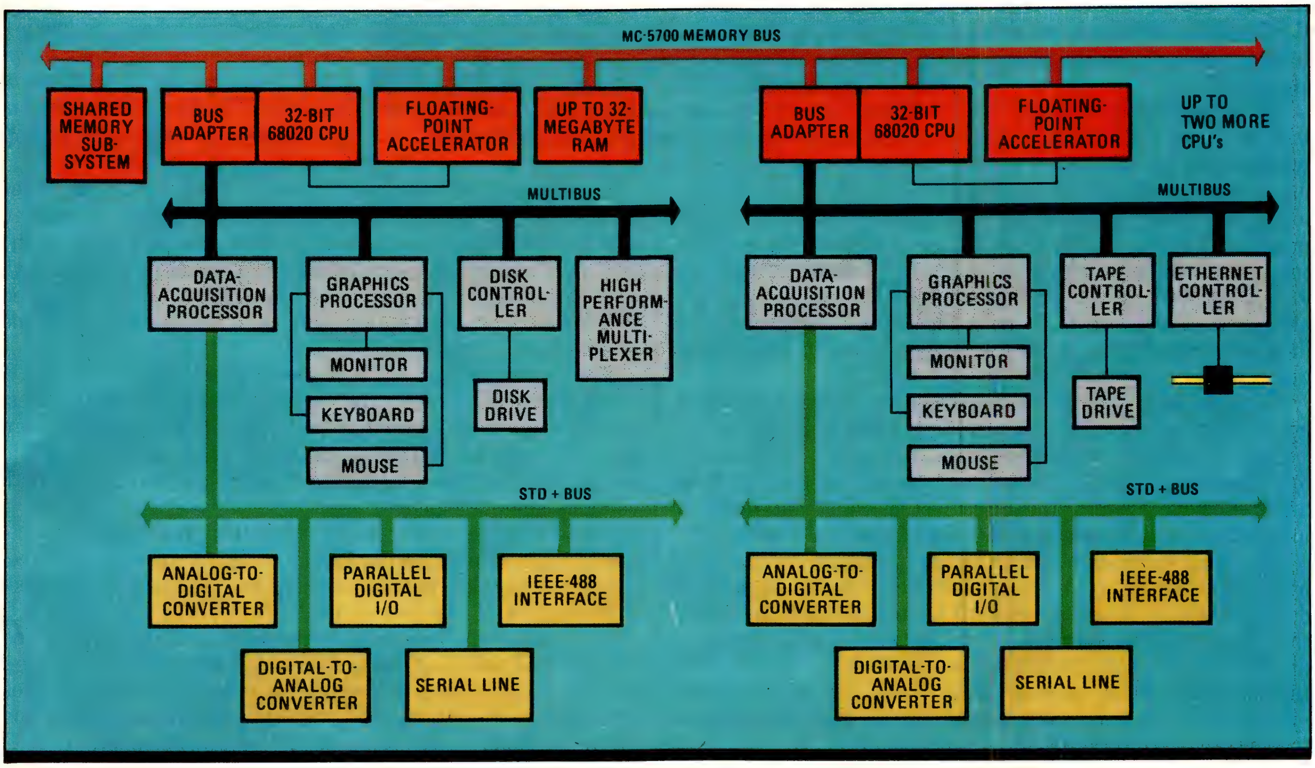
In a demanding real-time data-acquisition and -control application, massive amounts of data must be captured quickly without loss by the computer while it is processing previously acquired data and generating control signals for instruments, sensors, or actuators.

A fast memory subsystem alone cannot ensure this. Efficient assistance in floating-point computation is also required and is as integral a part of the 5000 family as it was of the earlier Masscomp systems.

Masscomp engineers also retained the data-acquisition processor and its STD+ bus from the previous system. It provides the fast data acquisition that is required in real-time systems and for which Masscomp systems are known.

Again, though, the system designers needed to speed up the floating-point unit to keep up with the 68020. So they rede-

2. BIG BROTHER. Details of the largest member of the 5000 family, the 5700, show the shared memory, the multiprocessor, and three tiers of buses. The memory bus ties the processors and the shared memory together. Several Multibuses handle the input/ouput devices.



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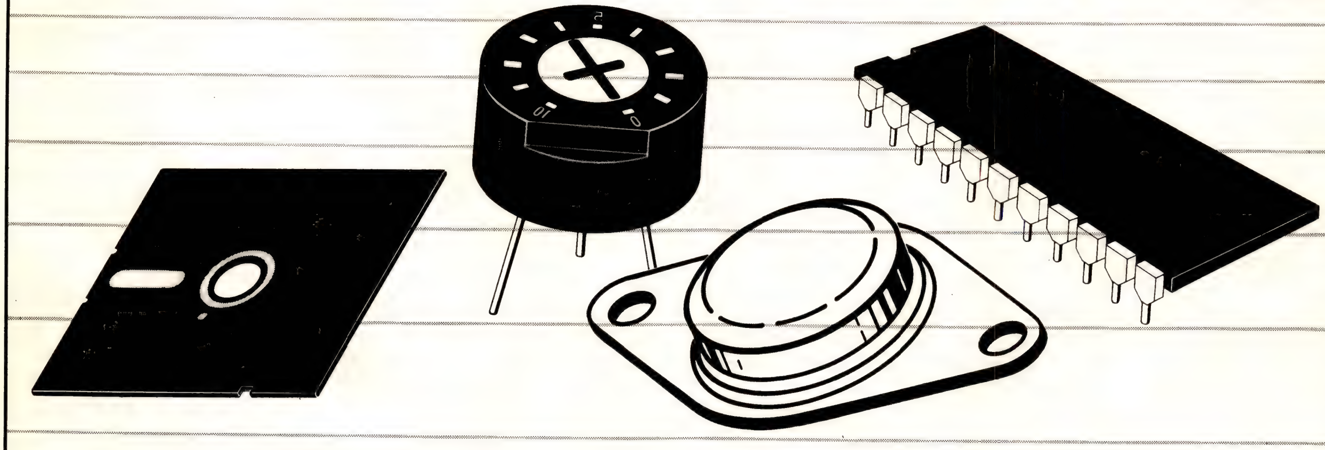

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tion of amorphous silicon and GaAs cheaper and more responsive to specific applications. Improved guidance and more precise manipulators on automated assembly lines have also led to better techniques for small-geometry etching and in addition can supply a more rugged packaging for semiconductor wafers.

Photovoltaic circuits are formed by printing a metalic paste onto the back of the wafer, drying it, then printing another metalic paste onto the front, forming a grid pattern. In a two-level, 1-μm-geometry design, the amorphous silicon serves as a passive transport switch that allows standard commercial chips to be wire-bonded to a 4-in. wafer. The interconnections are passive but easily reprogrammed and linked to each other with amorphous-silicon antifuses, which are resistive elements fabricated in the off-state at 200 MHz; an electrical pulse switches them to the on-state at 10 MHz.

The user can circumvent a bad circuit connection by simply blowing a bad antifuse and turning on a good one. Future developments could lead to an actively switched network, with amorphous silicon a strong contender as the material of choice.

Even without the wafer-scale connections, amorphous silicon serves as a better passivation material for the surfaces of semiconductor materials than does silicon dioxide, Little says. In addition, no new techniques are necessary for its use, so the underlying circuitry does not have to be redesigned.

A NEW CLASS OF HYBRIDS

Both the photovoltaic and semiconductor industries are striving for the same goals. For example, the wavelength of the etching energy, usually visible light, limits the development of submicron-circuit pathways. Thus most companies in semiconductor R&D are investigating short-wavelength X-ray deposition for submicron lithography for both photovoltaic and microelectronic processes.

"The most promising substrate material for X-ray lithography is gallium arsenide," says Little, "although it's only in the research stage for photovoltaics because we can't justify the cost of GaAs in energy applications." But Little also stresses that Spire's efforts to make GaAs competitive as a photovoltaic energy producer can easily be transferred to microelectronics. The inherent promise of GaAs is the high electron mobility associated with the material, making it about 20% efficient as a current carrier. This compares with an efficiency figure of about 15% for silicon.

Spire officials have identified three markets in the electronics industry for its GaAs products. They will suit electro-optics uses such as lasers, sensors, and telecommunications gear. Microwave equipment as well as superlattice ICs could also take advantage of GaAs technology. The company recently achieved the first reported epitaxial deposition of high-quality single-crystal GaAs directly on silicon substrates. Its metal-organic chemical-vapor-deposition system, the SPI-MO CVD 450, grows epitaxial layers of III-V compounds. The system offers both the reproducibility and flexibility to satisfy the needs of users involved in either research or production of semiconductors—mostly for photovoltaics but also for wafer-scale microelectronics (Fig. 1).

The system could lead to versatile hybrid circuits, according to Little. The technique will accomplish this by permitting the fabrication of monolithic structures in which the underlying silicon functions as an active component for internal microelectronic processing. Meanwhile, the GaAs, which can be used as a light emitter, will provide the optical link to the outside world, Little says.

The heart of the system is the reaction chamber, a water-cooled vessel and rotating vertical-geometry susceptor designed to achieve uniformity and reproducibility of thickness, doping, and composition. Also essential to the CVD 450's operation is the flexibility of the computational intelligence that runs it. A standard IBM Corp. Personal Computer is connected to a Westinghouse Corp. Numa-Logic programmable controller, through which an operator can define and document all aspects of the fabrication process.

GaAs-SILICON SUPERLATTICE

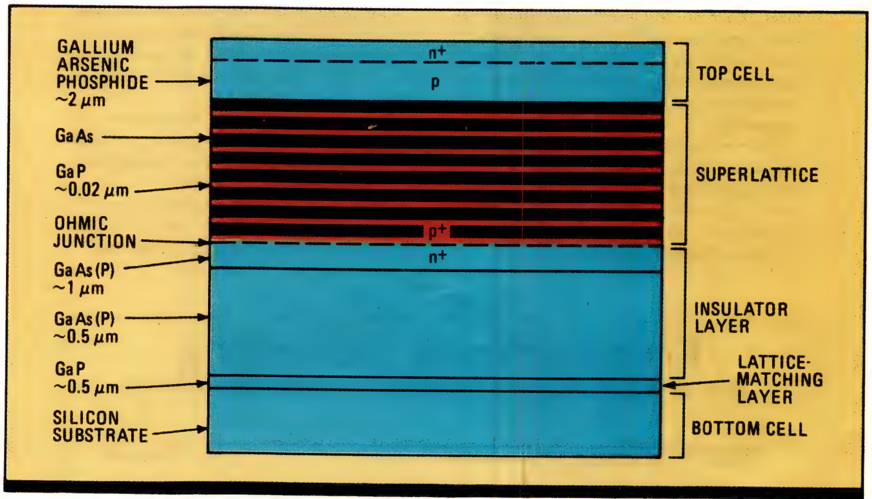
The user has considerable latitude to modify the controlling software, Little emphasizes. For example, software-driven temperature control allows abrupt doping and composition changes to be made while a crystal is growing. Thus the same machine can be used to produce semiconductors for a variety of applications.

With the CVD 450, the company plans to fabricate a highly efficient GaAs concentrator cell that uses external lenses to amplify the light impinging on a 1-cm^2 wafer. Researchers have demonstrated successfully in the laboratory a cell whose energy output equals more than 20% of the energy of the incident photons. Commercial availability is set for 1988. Processed with microelectronic circuits, such a cell would lend itself to fast low-power computation.

That level of efficiency is not an absolute necessity for the electronics industry, however. Similar, less efficient products are even closer to realization. One of the more promising is a superlattice based on a monolithic GaAs cell alloyed with phosphorous, layered over a low-band-gap silicon cell (Fig. 2). Superlattices are semiconductors in which two materials with different electronic properties are interleaved in very-thin alternating layers.

High-speed microprocessors as well as highly efficient photovoltaic cells could be designed around such lattices, and Spire is trying to enlist interest in this approach from both the energy industry and supercomputer manufacturers. Such a lattice mitigates charge dislocations by confining them to planes normal to the crystal's direction of growth, putting more charge where it is needed.

2. SUPERLATTICE. Submicron-geometry GaAs cells will provide more efficient electric power for photovoltaic applications and greater speed for microelectronics.



Spire is developing flexible manufacturing techniques that alter the widths of the interleaved layers, depending upon the GaAs alloy a customer chooses for his design. Eventually, the company could produce a device that would have ideal band gaps and lattice constants for a given material system—whether for photovoltaics or microelectronics. ☐

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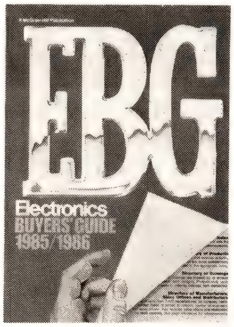

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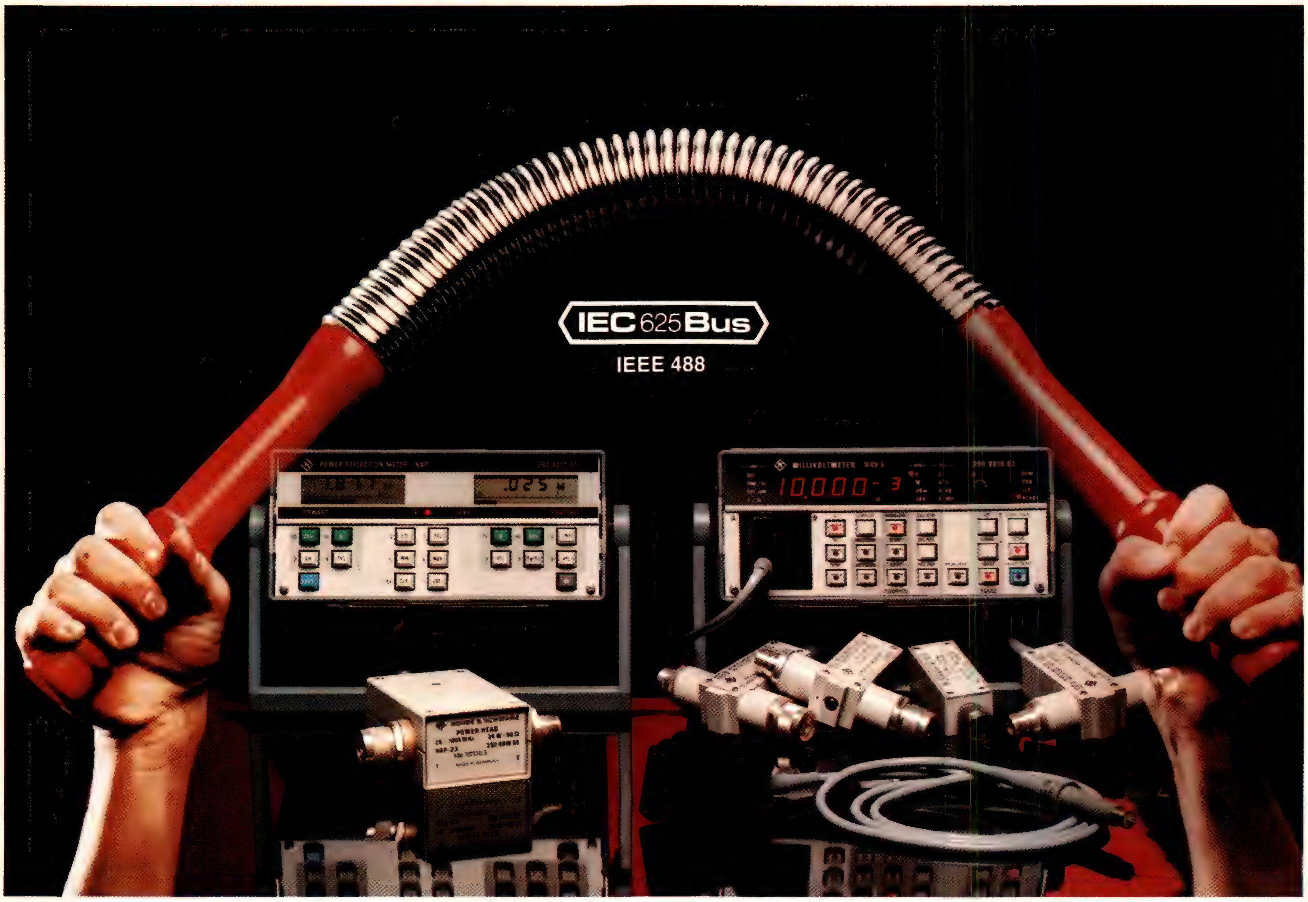

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PRODUCTS NEWSLETTER

TEKTRONIX SHIFTS CAE STRATEGY AND INTRODUCES NEW SOFTWARE FAMILY

Tektronix Inc. is shifting its computer-aided-engineering strategy. Instead of completing development of its 32032-based work station, which would have limited customers to one hardware base, the company is introducing a family of design software applications called WorkSystems. The packages will run on 80% of the computers now being used in such applications—machines from Apollo Computer Inc. and Digital Equipment Corp. as well as the company's own TekStation, an enhanced IBM Personal Computer AT. The eight WorkSystem packages are linked by a common data base and contain vertically integrated electronic tools for designing gate arrays, standard cells, custom ICs, as well as for developing software and testing designs. They will be marketed by the Tektronix CAE Systems unit. ☐

NOW IBM PC USERS CAN GET A 256-K-BYTE PLUG-IN MEMORY FOR $99.95

A 256-K-byte memory card designed for IBM Corp. Personal Computers and their compatibles is coming to market with two big guns: small size and small price. Built with 256-K chips by the Turner Hall Publishing division of Symantec Corp., the card will sell for $99.95 and takes up only half a card slot. Comparable cards built with 64-K chips now sell for more than $200. The 5-in.-square card fits into the short slot of the PC and comes with clock and calendar. The card will be sold by mail order. ☐

ZILOG SOUPS UP ITS TRIED-AND-TRUE Z8 8-BIT MICROCONTROLLER

Zilog Inc. is souping up its popular Z8 microcontroller by adding on-chip direct-memory-access circuitry and more than doubling the on-chip 8-bit registers—up from 128 to 272. The Super 8 is built with n-MOS technology and will run at 14 MHz, up from the Z8's 12 MHz. But next year the Exxon subsidiary plans a 20-MHz CMOS version. The new chip is aimed at such applications as optical-disk drives, Winchester disk drives, and high-speed modems, and printers. The bigger register set will make it feasible to use registers for on-chip storage. The chip will sell for $10 each in large quantities when Zilog reaches full production in the first quarter of next year. ☐

CONVEX MINISUPERCOMPUTER GETS SUPERCHARGED TO WORK EVEN FASTER

ZeroOne Systems Inc. has supercharged the Convex C1 computer so that it can function as a front-end processor to a Cray supercomputer or as an entry-level Cray compatible. The enhancement of Convex Computer Corp.'s C1 [*ElectronicsWeek*, Oct. 29, 1984, p. 17] includes the Hyperchannel link for Cray-like communications speeds and disk drives that are formatted to provide a "high degree of Cray disk- and file-system compatibility," ZeroOne says. The enhanced system will sell from $1 million to $1.5 million. ☐

MACHINE-VISION COMPANY JOINS RACE TO AUTOMATE SURFACE MOUNTING

A machine-vision system maker has added a new twist to surface-mounting automation. Synthetic Vision Systems Inc. has come up with a prototype that inspects the solder or paste dots laid down on a substrate before components are placed. Called Cyto Jr., the unit is a scaled-down version of the company's $200,000 TFI-4000 system for thick-film hybrid-circuit inspection. The prototype can inspect a 3½-by-3½-in. substrate containing eight hybrid circuits in about 5 s, checking that all solder dots are in the right place and within acceptable tolerances. The first system is scheduled for delivery to Ford Motor Co. by year end. Commercial versions of Cyto Jr., priced from $25,000 to $50,000, will be available later next year. ☐

ever, Chips and Technologies says it will develop a second phase of the PC AT-compatible Chipset in 1986 that will integrate the remaining LSI microperipherals and glue logic on the PC AT board.

Chips and Technologies is quoting November availability for the chip sets. In lots of 100 sets, the PC AT-compatible Chipset goes for $72.40 each; the Enhanced Graphics Chipset sells for $85.40 each. *–Eve Bennett*

Chips and Technologies Inc., 521 Cottonwood Dr., Milpitas, Calif. 95035. Phone (408) 434-0600 [Circle reader service number 338]

CHIPS SHOULD HELP PUSH MOVE TO OPTICAL STORAGE

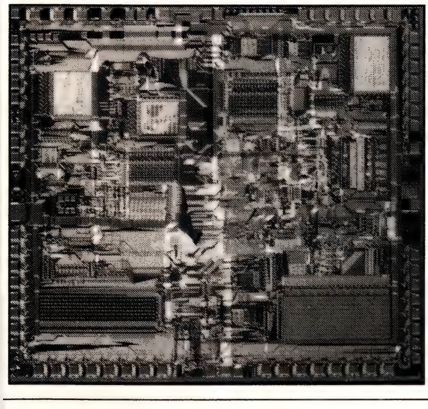
A document compression and expansion processor from Advanced Micro Devices greatly reduces requirements for document-storage capacity on magnetic or optical disks. The Am7970—a system on a single chip—sports three separate processing engines and a two-bus architecture on an n-MOS die. The chip should help push the move to optical storage.

The three engines—central controller, compression processor, and expansion processor—work together to quickly reduce the number of bits necessary to transmit or store black and white documents. The very large-scale IC achieves document compression and decompression by reducing redundant data in compliance with the standards set by the International Telegraph and Telephone Consultative Committee.

Using CCITT-compatible compression algorithms, the 7970 processor can reduce data representing bit-mapped, two-tone images from 5× to 50×. The processor can compress an 8½-by-11-in. document in 1 to 2 seconds. Its throughput is between 2 and 8 Mb/s running at its maximum 5-MHz clock rate.

The 68-pin processor is aimed at a variety of document-processing applications, including facsimile transmission systems, local networks in the office, and electronic file storage, such as optical laser disks. The compression-expansion processor will typically place 15 times more documents on magnetic and optical disks, estimates John Landau, product marketing manager at the company's Austin, Texas, facility. Currently, an 8½-by-11-in. document scanned at a resolution of 300 by 300 dots per inch requires about 1 megabyte of storage.

PROMISING. AMD's triple-engine n-MOS chip will push the move to optical storage.



The VLSI circuit contains a dual-bus architecture, which is designed to eliminate bus contention during the memory-intensive compression and decompression of documents. The chip has a central processing bus and a secondary local-document store bus.

DUAL-BUS ARCHITECTURE. Each bus can deal with 16 megabytes of storage, for a total of 32 megabytes of direct memory access. The 7970 also has a dual-bus direct-memory-access controller. In addition, the dual-bus architecture allows the chip to simultaneously expand and reduce the text and image data using separate processing steps.

The 7970 supports one-dimensional processing of data (one line at a time) for the highest throughput, using a modified Huffman run-length code. The chip's two-dimensional processing on redundant data (both horizontally and vertically) achieves the highest compression rate, using a modified read code. Both one-dimensional and two-dimensional compression techniques comply with the CCITT's group-3 and -4 standards.

The n-MOS circuit operates from a single 5-V power supply. It dissipates 2 W typical running at 5 MHz. Its temperature range is 0°C to 70°C.

In 100-piece quantities, the 7970 sells for $245 each in 68-pad ceramic leadless chip carriers. The company began making its first volume deliveries this month, and parts are available from AMD's distributors. The debut of the compression-expansion processor is the first entry in AMD's product-introduction-a-week campaign. The aggressive product-introduction blitz will start this week and continue for a year [*Electronics*, Sept. 16, 1985, p. 12]

By year end, the company plans to make available for loan to potential customers a plug-in expansion board, containing an Am7970 processor, for IBM Corp.'s Personal Computers. Designers can use the board in early system development. *–J. Robert Lineback*

Advanced Micro Devices Inc., 901 Thompson Place, P. O. Box 3453, Sunnyvale, Calif., 94088.
Phone (512) 448-5255 [Circle 339]

PLUG-INS ANALYZE LOGIC IN RANGE OF COMPUTERS

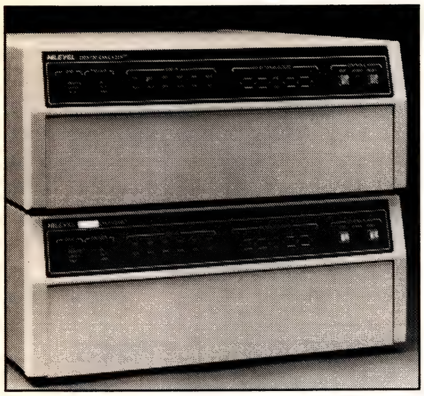
Four new plug-in modules from Dolch Logic Instruments Inc. extend the applications spectrum of the company's popular Colt and Atlas logic instrumentation systems. The four units take the two systems in "widely contrasting directions in the range of tasks they perform," says Volker Dolch, chairman of the West German company.

At one end, the new plug-ins adapt the Colt and Atlas to such relatively simple jobs as analyzing the performance of virtually all 8-bit microprocessors, with which "the world is still replete," as Dolch points out. At the other extreme, they make the two systems suitable for analysis tasks in supercomputers, bit-slice designs, and high-speed buses. In between are serial-data and network analysis and applications involving 16-bit processors.

Dolch plans to introduce the units at November's Wescon show in San Francisco. It hopes they will strengthen the company's position in the worldwide logic-analyzer market, in which Dolch ranks third behind Tektronix Inc. and Hewlett-Packard Co., with total sales expected to go to $18 million this year.

Dolch expects $6 million of that to be in the U. S., where the company has San Jose headquarters. It checks in as the fourth largest supplier of logic analyzers in the U. S., behind Tektronix, HP, and Gould Biomation. The well-established Colt and Atlas instruments account for about three quarters of the company's U. S. sales.

The first of the four plug-ins is the Trace unit, model 96100-48. This is a complete logic analyzer offering 48 channels of synchronous or asynchronous recording at up to 100 MHz. Because of its high speed on all channels,



Very High-Speed Integrated Circuits program. Models come in 25-, 35-, and 50-MHz speeds.

The DTS3700 series provides a combination of stimulus, logic analysis, and real-time comparison. Each of these sections can be configured in 16-bit (or pin) increments up to 256, letting the test system support up to 256 bidirectional or 512 unidirectional pins.

The 50-MHz model can store up to 4,096 stimulus vectors; at lower data rates, the system provides up to 16-K of stimulus vectors. The logic analyzer section supports devices that require data-acquisition paths of up to 256 channels, synchronizing acquisition with up to 16 clocks simultaneously.

Available 4 to 12 weeks after ordering, the systems start at $30,000.

Hilevel Technology Inc., 18902 Bardeen,
Irvine, Calif. 92715.
Phone (714) 752-5215 [Circle 371]

COMPUTERS RUN UNIX ON MULTIBUS

The DataSeries family of high-performance microcomputers—the eight-user DataMate, 16-user DataManager, and 32-user DataMaster—all use Multibus architectures and run under Unix V with RM/COS as an alternative operating system. All are equipped with the 68010 microprocessor.

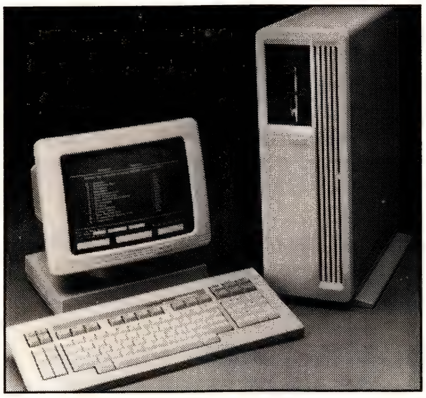
On the DataMaster, the most powerful member of the series, the standard configuration includes 3 megabytes of on-board memory and 512-K bytes of Multibus memory. A 334-megabyte disk drive provides mass storage and 474-megabyte drives can be added.

An Ethernet controller board, two serial ports, and a parallel port are standard, as is a 15-slot Multibus card cage. Unite, networking software to support 32 users, sells for $2,800. The price of the DataMaster is $28,995, the DataMate is $11,750, and the DataManager is $15,995. The systems are available now.

CYB Systems Inc., 2215 W. Braker La.,
Austin, Texas 78758.
Phone (512) 835-2266 [Circle 374]

COMPUTER CAN BE CLUSTER CONTROLLER

Power 5/32, an office computer that can also perform as a cluster controller, uses the hardware-intensive memory-management scheme originally created for the company's Power 6/32 32-bit superminicomputer. The Power 5/32 runs under Unix 4.2bsd; its CPU is built around the 16-bit 68010 microprocessor, and a basic system offers 2 megabytes of parity-checked main memory expandable to 4 megabytes. Over two RS-422 ports and four RS-232-C ports, the Power 5/32 supports eight Powerterminal II work stations plus printers or other peripherals, including personal computers.



The storage subsystem supports one or two 85-megabyte disks and a 45- to 60-megabyte streaming tape drive for archiving. Disk and tape can be written simultaneously. Officepower software includes an electronic mail capability, and PTNet allows the Power 5/32 and the Powerterminal II to communicate at a 307-kilobaud rate; Omninet and Ethernet options are available. Prices for a typical system begin at $4,794 per user, with delivery scheduled for the fourth quarter of 1985.

Computer Consoles Inc., 97 Humboldt St.,
Rochester, N.Y. 14609.
Phone (716) 482-5000 [Circle 378]

BUFFERED DATA SPEEDS TESTER

The system 910 Tactician analysis package handles data from as many as 16 Factron test or rework stations because it uses a Z80 single-board computer to buffer data flow rather than tie up the 68010-based CPU. As a result, the testers are not held up waiting to transfer the data and production is maintained.

The Tactician package monitors all test and repair results in real time, tracking each board continuously. Then, from the failure data, Tactician generates reports that monitor process yield and track component quality. Under control of a data-base manager, the system also generates custom reports.

The basic Tactician system includes the 68010 microprocessor, 2 megabytes of main memory and a 50-megabyte hard disk—both expandable—and software protocol packages. A complete system, including terminals and hookup costs for the testers and rework stations, is $50,000. The delivery time will depend upon configuration.

Factron/Schlumberger, 1 Fairchild Sq.,
Clifton Park, N.Y. 12065.
Phone (518) 877-7042 [Circle 365]

SYSTEM ALIGNS, TESTS SSB RADIOS

A telecommunications test system, the Adate WJ-1570, performs automatic alignment and performance evaluation of digital and analog single-sideband microwave relay radios and multiline channel-switching systems. It operates from dc up to 6 GHz.

A turnkey system, the WJ-1570 includes the main rack assembly, an umbilical cable assembly, and a remote test interface that may be positioned up to 50 ft away from the rack by means of the cable. System software that runs under AT&T Bell Laboratories' Unix is also part of the package.

The WJ-1570 uses off-the-shelf instruments for test and measurement. Data is stored on a 65-megabyte Winchester hard-disk drive backed by a 75-megabyte streaming-tape-cartridge subsystem. Price and delivery information were unavailable at press time.

Watkins-Johnson Co., ATE Applications
Engineering Division, 2525 N. First St., San
Jose, Calif. 95131.
Phone (408) 262-1411 [Circle 366]

STATION TESTS COMPONENTS, WAFERS

For use in failure analysis or quality control, the REL-4100A analytical probe station accepts either packaged components or wafers measuring up to 6 in. The system's barrel-driven stage has a resolution to within ±1 μm and is accurate to within ±0.0001 in. over the entire travel distance, making the system capable of submicron probing. All movements are free from backlash, the manufacturer says.

The X-Y stage is available with a 1-μm digital readout with a 166-location memory. The probe platen will accommodate up to 12 micropositioners that can be raised simultaneously, then moved to the next device under test and dropped to within 1 μm of the same fixed probe pattern.

Options for the REL-4100A include probe-card holders, ultrasonic cutters,

LETTERS

Old technologies never die

To the editor: I'm sure the power-tube industry is thankful for the University of Maryland's Victor Granatstein and Robert Parker of the Naval Research Laboratory [*Electronics*, Sept. 2, 1985, p. 34]. Here are two independent people who see the need to bolster an industry that is ignored to some degree because it is based on an "old technology."

We germanium people know the feeling. Germanium semiconductor technology survives, as I'm sure the power tube will survive, simply because there are too many applications and designs that must use these products. Other technologies just don't perform.

Granatstein's statement, "I think the power of solid state has peaked out," is food for thought. Although he was referring to the power tube versus solid state, I think the statement is interesting when applied to other types of electronic devices that supposedly "have seen their day" and yet continue to have a place in today's electronic designs.

It is interesting that state-of-the-art applications—space radars, electronic countermeasures, and satellite communications systems, to name a few—will use power tubes that some sources say should be replaced with solid state. Well, the same equipment will probably have germanium semiconductors, photodetectors, rectifiers, and so on.

Richard Kassiotis
Sales Manager
Germanium & Power Devices Corp.
Andover, Mass.

Getting into the picture

To the editor: I found your articles on picture phones very interesting [*Electronics*, Aug. 19, 1985, p. 30, p. 34, p. 36]. My company has several video digitizers, monochrome and color—some in prototype and others in production.

Two of our products, the Apple Frame Grabber and AFG II, are standalone cards that digitize any NTSC video source from video recorders, cameras, or live TV in 1/60th of a second per frame directly into any Apple computer's 8-K memory page. Therefore if the digitizer is directed to digitize into the computer's video display memory, you can watch digitized video in real time.

Mike R. Moore
President, Micro Mainframe
Rancho Cordova, Calif.

Correction

Two photos were inadvertently switched in the Sept. 23 issue. The right-hand photo on p. 30 is actually Clinton Kelly; the right-hand photo on p. 31 is Brian Oakley. *Electronics* regrets the error.

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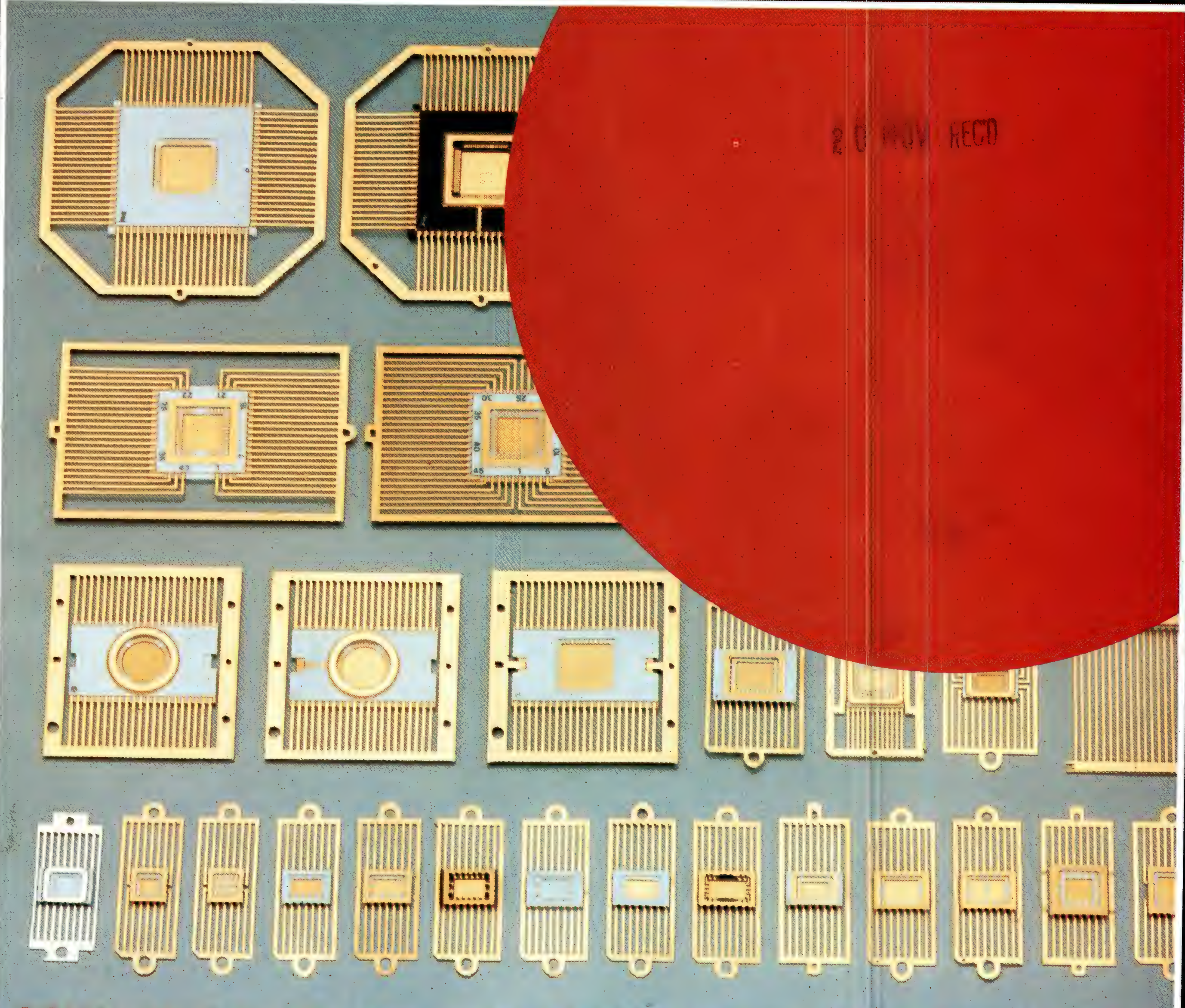

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CONSUMER PRODUCTS, SUPERCOMPUTERS DRIVE INNOVATION
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WHY JAPANESE ARE PARING CHIP-MAKING PLANS IN U.S./45

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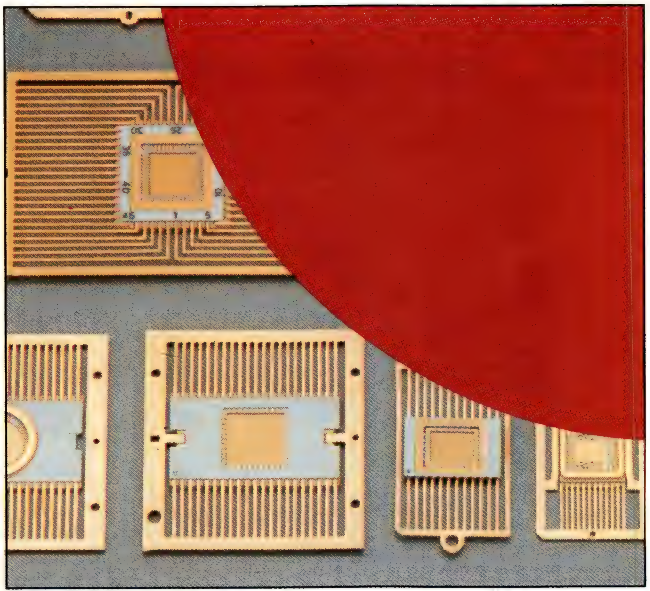

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PUBLISHER'S LETTER

It is safe to say that no American journalist has better contacts among the officials of Japanese electronics companies than our Charlie Cohen. In January, he will mark his 20th anniversary as *Electronics'* man in Tokyo, which would probably make him the dean of the U. S. press corps there if such records were kept officially.

VETERAN. Cohen nears the 20-year mark.

Charlie earned an MSEE from the University of Tokyo to go with his bachelor's degree from Cornell University. And during his student days in Tokyo Charlie numbered among his fellow students many of the men who today sit in the executive suites of the biggest electronics companies in Japan.

Charlie modestly insists that he has an "uninteresting résumé because I have been in one place that long." But that's not exactly the case: consider the way he got to Japan in the first place.

Charlie was in the Army, stationed at Fort Monmouth, N. J., when, as he tells it, "I entered Japan in the fall of 1955 after volunteering to replace a guy who had orders to go to Japan in one hand and a crying wife in the other. It seemed like a good way to get out of Fort Monmouth and put a little interest in my life."

After being discharged and completing his graduate work, Cohen went to work in Tokyo for McGraw-Hill World News, the global service that helps provide news coverage for McGraw-Hill magazines and newsletters. "I started stringing for World News in 1961 and working full-time that same year. Then I switched to *Electronics.*"

Life in Japan can have its complications. Although Cohen does most of his reporting in Japanese, he writes only in English; he has written almost nothing in Japanese since he left school. And then there is what should be the relatively simple matter of buying a personal computer. "I desperately wanted to buy a Japanese computer for Japanese-language word processing," he says. "But the incompatibility of Japanese computers with each other and with U. S. software made an American computer seem a better bet."

But even without the Japanese writing, Cohen still manages to combine his engineering education, journalistic talents, and intimate knowledge of Japan and the Japanese to do a remarkable job of covering the electronics industry there. The latest example is this week's cover story on Japanese advances in packaging, which begins on p. 26.

Two of our most popular features—the annual Technology Update and Market Report and Forecast—are being offered in a single reprint to be available in January. Send a check or money order for $10 to *Electronics,* 1221 Avenue of the Americas, New York, N. Y. 10020.

Laurence Altman

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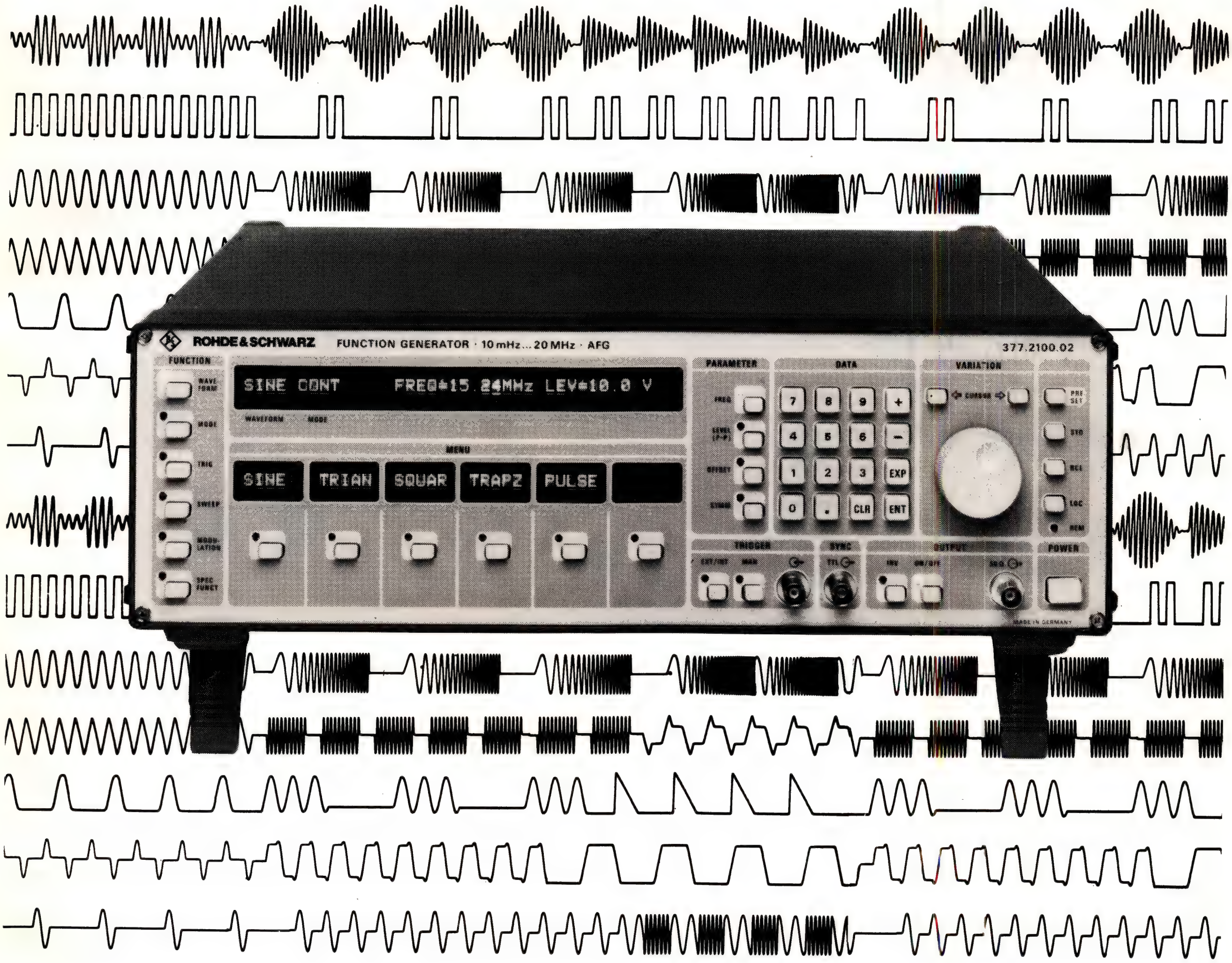

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NOVEMBER 11, 1985

TECHNOLOGY NEWSLETTER

SCOTTISH SILICON COMPILER TO BEGIN DESIGNING COMMERCIAL CIRCUITS

Work will begin shortly on the design of high-performance signal-processing circuits aided by a silicon compiler developed four years ago at Edinburgh University in Scotland. Wolfson Microelectronics Ltd., a commercial spinoff of the school, extensively modified the compiler for commercial applications. Called First (for Fast Implementation of Real-time Signal Transforms), the compiler assembles a high-level functional description of the custom circuit on finished mask tapes, using a library of parameterized bit-serial digital signal-processing operators [*Electronics*, July 28, 1982, p. 68]. First had originally turned out custom circuits quickly and accurately for the university, but it used a slow n-channel process and its channel-routed architecture used silicon inefficiently. Scientists at Wolfson re-engineered the compiler in order to add parallel digital cells, including a bit-slice processor. They also converted to a 2-μm double-layer-metalization process developed by Plessey Co. And to improve packing densities, cells are now placed manually and routed automatically with the aid of Wolfson's MiDAS design system. This features geometric editors, cell and chip assemblers, as well as standard circuit and logic simulators. First's first circuit will be a 128-point finite-impulse-response filter. □

MICRON TECHNOLOGY ABOUT TO INTRODUCE 1-Mb CMOS DRAM

Look for Micron Technology Inc., the Boise, Idaho, maker of dynamic random-access memories, to introduce a full 1-Mb CMOS DRAM at next week's Wescon in San Francisco. The part will be faster than 100 ns and will come with two organization options: 1 Mb by 1 bit and 256-K by 4 bits. A company representative says Micron plans next year to cluster four such RAMs on a single silicon chip, interconnected by a metal layer, to implement a 4-Mb part. Hamming code incorporated in each DRAM will correct errors caused by defective bits. □

A RUGGED CASE ENABLES MAXELL BACKUP CARTRIDGES TO RUN FASTER

Memory backup cartridges will run up to three times faster than other tape cartridges, thanks to the ruggedness of a fiberglass-impregnated molded plastic case developed by Maxell Corp. 3M Co. is the only other supplier of such products. The Moonachie, N. J., magnetic-media maker is rolling out two high-speed, high-capacity, magnetic-tape cartridges in 20- and 25-megabyte versions at Wescon in San Francisco next week. About the same size as standard audio cassettes, the cartridges can run at speeds of 180 to 220 in./s. Designed as backup for Winchester and floppy-disk drives, the cartridges will sell for $7 to $9 on an original-equipment-manufacturer basis. Maxell will also be pushing for a new standard at Wescon: a 2½-in. floppy disk that comes in a rigid housing for the small portable computers known as electronic notebooks. Maxell says Epson America Inc. already supports the standard and will make drives for the 1-megabyte disks. □

EUREKA LAUNCHES 10 DEVELOPMENT PROJECTS

Eureka, the French initiative to promote European cooperation in high technology, got a boost last week when both the British and West German governments indicated they would give it financial support. And at the same Hanover organizational meeting, the first 10 Eureka projects were approved. They include developing an amorphous-silicon computer chip, a compact vectorial computer, a European standard personal microcomputer for home and educational uses, and a data-processing and telecommunications network. □

NOVEMBER 11, 1985

ELECTRONICS NEWSLETTER

DATA GENERAL ABOUT TO LAUNCH WORK STATION USING ITS EAGLE CHIP SET

Data General Corp. next week will roll out two products that are highly critical to its future growth. Both products, not surprisingly, will go up against machines from minicomputer rival Digital Equipment Corp. The Westborough, Mass., company will introduce a high-end 5-mips computer and a work station that is expected to use a micro-Eagle chip set incorporating the complete MV series instruction set. The high-performance computer system is an extension of the MV series that will compete with DEC's VAX 8600. Its architecture is implemented completely with Motorola gate arrays. The work station is expected to be positioned against DEC's MicroVax II and machines from Apollo and Sun. □

SILICONIX SET TO GO FOR BIGGER SHARE OF ASIC MARKET

Siliconix Inc. is going for a bigger share of the application-specific integrated-circuit market. The Santa Clara, Calif., chipmaker is expected to make a major announcement this week on its increased ASIC capability. It plans to attack the commercial gate-array market with a new technology from an outside supplier suitable for high-density commercial chips. For the past two years, Siliconix has been selling low- to medium-density (180- to 2,400-gate) arrays in the military market. These circuits are made with 3- and 5-μm technologies and operate at clock rates up to 50 MHz. □

JAPANESE MINISTRY GRANTS IBM LICENSES TO PATENTS

Japan's Ministry of International Trade and Industry on Nov. 1 granted IBM licenses to more than 700 data-processing-related patents owned by the Japanese government [*Electronics,* Aug. 5, 1985, p. 12]. A representative of the Agency of Industrial Science and Technology, which manages the patents, says all the patents are for inventions at six companies involved with large government-sponsored projects and research. IBM has cross-licenses with all six, he explains, and wanted the rights to their inventions that it heretofore did not have access to. The five-year agreement calls for all royalties to be paid to the Japanese government, which will receive an undisclosed percentage of sales. Similar deals may open up to other U. S. firms. □

DISAPPOINTED SOUTH KOREAN VCR MAKERS TRIM PRODUCTION

Disappointing sales of their video cassette recorders in the U. S. and Europe have derailed the plans of South Korean makers to capture a 3% world-market share in their first year of full-scale exports [*ElectronicsWeek,* April 15, 1985, p. 22]. South Korean makers, which expected to ship 1.5 million units this year, have delivered only 566,000 VCRs through August and are cutting back production. Gold Star, Samsung Electronics, and Daewoo Electronics last month each cut their monthly output to 60,000 units, less than half the capacity of the three Seoul VCR makers. Falling retail prices—the average price of a VCR in the U. S. has dropped to about $290, down from about $400 a year ago—have added to their difficulties, the Koreans say. □

AS EXPECTED, INTEL ENTERS PROGRAMMABLE-LOGIC MARKET

Intel Corp. made its long-awaited entry into the programmable-logic market last week, introducing two erasable products and a family of programming tools. The chips, 600- and 1,200-gate parts, and the tools, a development system for programming and testing, derive from technology that Intel developed jointly with Altera Corp., Santa Clara, Calif. Altera already has been marketing the chips, which are built with Intel's 33-MHz CHMOS process. □

NOVEMBER 11, 1985

PRODUCTS NEWSLETTER

TI 8-BIT MICROCOMPUTER HAS ON-CHIP EPROM

One of the three new 8-bit microcomputer chips Texas Instruments Inc. will add to its four-year-old TMS7000 family this week has on-chip EPROM. The n-MOS TMS7742 offers 4-K bytes of EPROM, 256 bytes of RAM, a serial port, and three timers. It sells for $38.40 each in 100-piece quantities. A mask-ROM part, the 7042, comes with 4-K bytes of ROM and sells for $7.68 in 10,000-piece quantities. The third chip, the 7002, is a ROM-less version that sells for $8.95 in 1,000-piece lots. In the coming months, look for the Dallas company to introduce a totally new single-chip microcomputer design, dubbed Roadrunner, that will have EEPROM. ☐

A FACTORY WORK STATION FROM INTEL ACCEPTS VOICE INPUT

Three new speech-recognition products from Intel Corp. will give the worker easy input into factory computers. The iSWS100 work station accepts voice input and passes the data on to the iSWS540 speech-cell controller. The latter coordinates the work stations' activities, analyzes data, and generates data in a form compatible with the Manufacturing Automation Protocol. The $19,000 work station will be available next month; the $35,000 controller will start shipping in January. The third member of the trio, the $15,000 iSWS090 speech-development system, is available now. ☐

DEC DRAWS OTHER VENDORS' PRODUCTS INTO ITS CIM LOOP

A software package from Digital Equipment Corp. opens up the computer-integrated-manufacturing loop by tracking changes in design data and moving them over an Ethernet among different vendors' hardware and application packages. The Maynard, Mass., company's system goes a step beyond similar systems that operate only with a single manufacturer's products. The Engineering Data Control System runs on DEC's VAX-11 computers. ☐

68000 RECALIBRATES MARCONI'S SWEEP GENERATOR

A programmable sweep generator from Marconi Instruments Ltd. uses a 68000 microprocessor to speed recalibration. Instead of recalibrating every 8 hours as is conventionally done, the 6310 can do the job every 15 minutes. This gives a frequency accuracy during the sweep of ±20 MHz typically and a leveled power accuracy of ±0.2 dB. The instrument stores up to six front-panel settings; it directly controls the yttrium-indium-garnet oscillators, automatically compensating for frequency nonlinearities. The 6310 can connect over an IEEE-488 interface bus to Marconi's automatic amplitude analyzer to monitor the performance of amplifiers, filters, and other communications gear. ☐

MULTIFUNCTION CARD EXPANDS IBM PC'S MEMORY UP TO 1.5 MEGABYTES

The PS, Intel Corp.'s latest multifunction board in its Above Board series for IBM Personal Computers expands memory on IBM PCs up to 1.5 megabytes above the usual 640-K-byte limit. Additional functions on the board, which comes from the company's Personal Computer Enhancement Operation in Hillsboro, Ore., include two I/O ports, a clock-calendar, a RAM that acts as disk, and print buffer. The 64-K-byte version, expandable to 348-K bytes, costs $445, and the 256-K-byte version, expandable to 1.5 megabytes, sells for $545. The PS conforms to Revision 3.2 of the Expanded Memory Specification devised by Intel, Lotus, and Microsoft. EMS allows the expansion of memory on IBM PCs up to 8 megabytes above the 640-K-byte that the machine can directly address. ☐

formance, as does Joseph P. Schoendorf, president of Industrial Networking Inc., a Santa Clara, Calif., joint venture between Ungermann-Bass Inc. and General Electric Co. "We'll support both [EPA and the full seven-layer architecture] on our carrier-band products, but we think most customers will go with the full functionality," says Schoendorf.

He disagrees with GM and others who say that MAP carrier-band implementations will lower MAP costs. "If you look at the total plant costs, there wouldn't be much difference in the cost of a plant wired heavily with carrier-band versus one done totally with broadband," he contends. "People forget that you need a bridge from the carrier-band subnet to the broadband MAP backbone," a factor he says will jack up carrier-band costs.

The MAP carrier-band approach was tested at Eastman Kodak Co. this spring. From those tests came a set of recommendations that are now being considered by the IEEE-802 committee [*Electronics,* Nov. 4, 1985, p. 55]. A final vote on the recommended extensions is scheduled for this month, says GM's Dezelan. She points out that the vote will deal only with signaling techniques and leaves a number of issues still to be resolved.

These include the minimum distance required between taps to avoid problems due to tap reflections, as well as the maximum number of nodes a carrier-band subnet can support. The Kodak group recommended a maximum of 32 nodes per subnet. *–Wesley R. Iversen*

TESTING

ON-CHIP TEST DESIGN GETS CLOSE TO ZERO DOPANTS

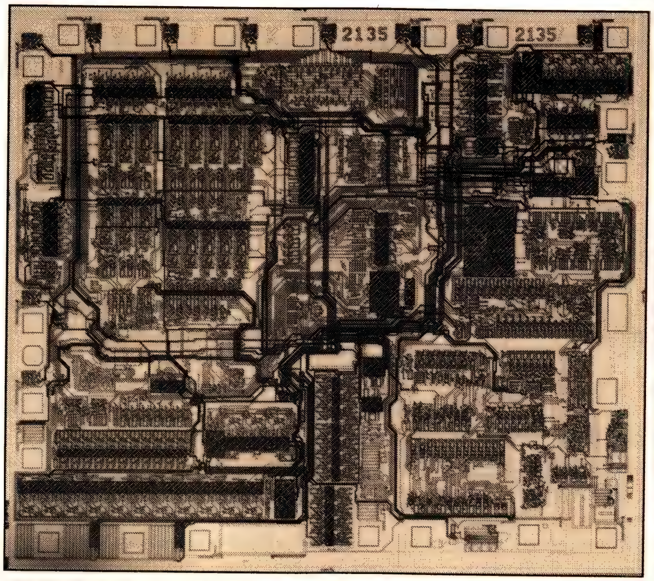
HEILBRONN, WEST GERMANY

Engineers at Telefunken electronic GmbH have combined a structured circuit layout with scan-path techniques to come up with a test concept that takes a big step toward pushing complex random-logic digital MOS integrated circuits to zero-defect levels.

Implemented with scan-path test circuitry integrated on chip, the technique achieves 99% fault coverage—that is, the number of detectable errors relative to the number of all possible errors is around 99%. That figure, the company says, compares with the 85% to 90% typical for standard IC test methods.

The new approach cuts test times at least tenfold. And when a failure is found, the test result localizes not only the defective gate or flip-flop, but also the input. In most cases, the input is responsible for circuit failures. Telefunken engineers are also developing ICs whose on-chip test aids check analog, as well as digital, functions.

Like other on-chip test strategies, the method adds to a chip's size. Depending on circuit complexity and the point in the design phase at which the test aids are integrated, from 15% to 25% more area is added. But the high fault coverage and the reduction in test time compensate for this drawback, claims Paul Sieber, MOS product development manager at the company's Heilbronn facilities.



TESTABLE. Test circuits (darkened areas) on an 11.9-mm^2, 5,000-transistor, data-transmission chip cut testing time from 360 s to 1.

Telefunken electronic, a joint venture of Frankfurt-based AEG AG and United Technologies Corp. of Hartford, Conn., brought the "concept's maturity to such a level that we will implement it in all future complex standard and custom random-logic digital MOS devices we produce and deliver," says Sieber.

First chips incorporating the method will be used in an infrared remote-control system for cars. Two years in development, the approach is based on a structured layout that partitions a chip into functional blocks, the implementation of a scan-path technique within the blocks, and an on-chip test bus.

The Heilbronn engineers incorporate the test aids into the chip during the early phases of its design. The IC is built up from a number of blocks that are as autonomous as possible and therefore can be tested either in parallel or independently. Each block is connected to the on-chip test bus.

Test-bus controls check the sequences and the transfer of data from block to block as well as between the chip and the external test system. By chaining the flip-flops into shift-register configuration, the scan-path technique reduces the test time from 2 to the nth power to 2n, where n is the number of flip-flops.

STATIC ONLY. The test method checks for static faults (nodes stuck at logical 0 or 1) and dynamic faults, which may be due to, say, errors in delay time. It cannot, however, keep track of faults due to parameter drift. "That's why demands for absolute zero-defect quality will not be fulfilled in the near future," says Werner Denner, head of Telefunken's Advanced Test Methods Development team.

In a complex chip, extra pins usually cannot be spared for test purposes, so the test-bus lines as well as those of the control logic must be multiplexed with whatever pins may be tapped. This limits the number of blocks into which an IC may be divided. A complex chip may have from 5 to more than 10 blocks.

To ensure that complex blocks can be checked out, each integrates the circuitry for the scan-path technique, a descendant of the level-sensitive scan design developed by IBM Corp. more than six years ago. Telefunken's scan technique chains all storage elements within the block to one or more parallel shift registers, which are connected to the external pins. All storage elements are thus accessible from the outside. The sequential logic is then reduced to combinational logic, which is easier to test.

To point up the benefits and the penalties of the Heilbronn test method, Denner's team compared a medium-complexity test IC (one with about 1,500 transistors on a 6.9-mm^2 chip) incorporating the test aids with an identical device without such aids.

The comparison showed that the test chip uses about 23% of its chip area for the added circuitry. This results in a corresponding drop in yield—a wafer would have 23% fewer chips. Further, the test chip calls for 774 nodes, about 280 more than the regular chip.

But this relatively high expense in real estate buys a big saving in test time and test preparation. Integrating the test aids slashed the number of test cycles required for the function tests nearly tenfold—

trator, would be required to select the technologies to be purchased and distribute the finished product.

"We would be putting one guy in the business to make buggy whips," Stensrude said. He expects to detail his proposal next month during a meeting with EIA and DESC officials.

EIA attorneys have no problem with Stensrude's plan, said John M. Kinn, the group's vice president. To meet procurement regulations, bids would likely have to be solicited from several foundries to make each product family.

At least one chip maker, Lansdale Transistor and Electronics, Phoenix, promotes itself as a "buggy-whip" maker. Since 1978, the company has purchased old chip lines, making it the preeminent supplier of discontinued parts.

"We push a win, win, win solution," said R. Dale Lillard, Lansdale's president. "Lansdale grows, chip manufacturers get a screaming monkey off their backs, and the customer has a long-term source of supply." During the current fiscal year, Lansdale will generate about $3.6 million, or 60% of its revenue, selling obsolete chips, some made on 3-in.-diameter gold-doped bipolar wafers.

What Lansdale wants is Washington's help to defray the cost of buying chip makers' know-how: it can cost as much as $1 million to acquire a major technology. "The overhead has to be spread," Lillard said. Government officials question the propriety of such a subsidy if a company is free to offer these older parts commercially.

A second solution, considered the simplest and most cost-effective, is called Life of Type buys. When a vendor informs DESC that a part is to be discontinued, DESC buys a lifetime supply.

Unfortunately, Pentagon officials "are not always notified or, if we are, it is frequently without enough time to develop reasonable reactive plans," said James P. Wade Jr., assistant secretary of defense for logistics and acquisition, in a recent letter to 124 suppliers. In the letter, Wade requested that each company give the DOD at least six months' warning before discontinuing production of a particular item. The major difficulty with Life of Type buys is accurately determining the volume required.

Under one plan, Pentagon would build old parts itself

The problem is magnified for foreign countries needing these short-lived parts to maintain hardware purchased from the U. S. government. After the manufacturers' grace period, they do not have access to DESC's stockpile.

Other questions that must be addressed include the effect of long-term storage on part quality and reliability, how to handle incoming testing, and whose needs take priority.

SUBSTITUTES. The second most cost-effective alternative is substituting similar parts. This is far from routine, however, because of the proliferation of vendor-specific chips in military hardware and the increasing complexity of devices.

A third alternative is to emulate chips, using sophisticated software tools to reverse-engineer them. The Navy and the Air Force have pilot chip-emulation projects under way. Though emulation provides chips that have the same form, fit, and function as the original, the high cost and long lead time required to produce working chips reduce its appeal.

The final option discussed at the conference was for the Pentagon to purchase older chip-making know-how from the producer and then turn out products on its own captive lines. Recently, the Navy Ocean Systems Center in San Diego undertook such an effort when it purchased Motorola's emitter-coupled-logic technology. Navy officials say that though their facilities can make replacement parts in a pinch, they are not in the chip-making business. *–Ira Breskin*

DISPLAY SHOWS 'HILL BEHIND THE HILL'

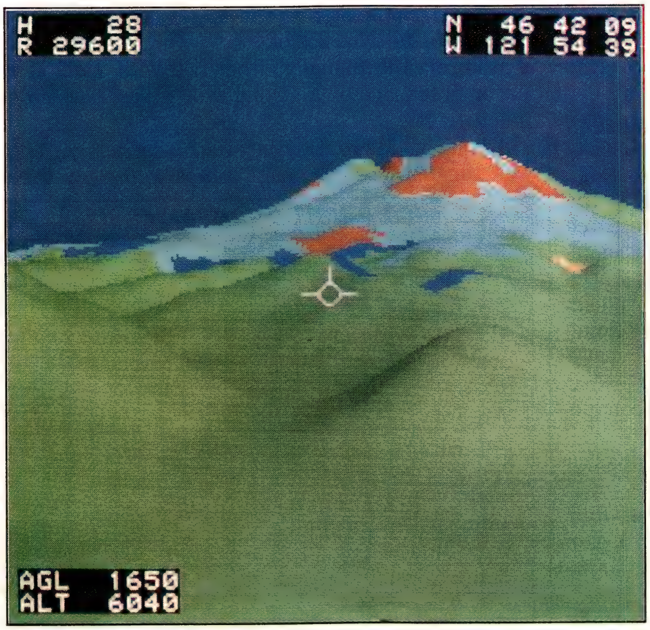
EL SEGUNDO, CALIF.

An eye-catching feature has been developed for experimental systems that store digital terrain data: a moving map displayed on monitors to help a pilot pinpoint his aircraft's position. Beyond its visual attractions, however, digitized elevation and terrain-feature information has potential for many kinds of military missions.

To get the upgraded performance that these applications demand, the Air Force has tapped Hughes Aircraft Co. to develop by late next year its Integrated Terrain Access and Retrieval System. Called "the next generation of digital mapping equipment" by one Air Force research and development official, Itars would push to the limits of present processing and mass-storage technology.

Hughes is working on Itars for the Avionics Laboratory at Wright-Patterson Air Force Base, Dayton, Ohio. The system will permit pilots to make big improvements in mission performance, believes Air Force project engineer Donald M. Small. "We are beginning a new era of avionic development," he says.

The technology "could have the biggest impact since radar," says Lt. Col. Donald H. Ross, who heads the advanced fighter-technology integration program at Wright-Patterson. "A pilot is no longer line-of-sight limited, but can see the hill behind the hill."



LOOK AHEAD. The Itars moving-map system will give pilots a perspective view of what's ahead, despite darkness or thick clouds.

Itars is charged with making "map data" more than just a means for generating graphic displays—although important display improvements are in the works also, explains J. William Weber, manager of Hughes's display-systems laboratory, a part of the company's Radar Systems Group. Itars also must integrate terrain data with avionic subsystems that handle flight control and weapons delivery.

In particular, such data must be provided to four subsystems aboard an aircraft: threat-avoidance equipment, especially useful for hazardous low-altitude missions where the pilot needs precise terrain data to dodge enemy sensors, terrain-following and -avoidance gear to augment radar, by January what steps to take. All top Intel managers will survey their operations and find areas to trim.

A representative said Intel had recently experienced a slight upturn in bookings and was optimistic that the slump had bottomed out. However, Intel expects a prolonged period of lower business performance that will affect its profitability, and so it is looking at ways to cut costs even further.

Texas Instruments Inc., like Intel, is looking to streamline operations. But TI is not abandoning the RAM business, because memories are vital technology drivers, says William N. Sick., president of TI's Semiconductor Group in Dallas.

One reason for the bad showing by U. S. companies versus Japanese producers is that "the U. S. market declined a lot more than the Japanese market," says F. Joseph Van Poppelen, vice president of semiconductor marketing for National Semiconductor Corp. The U. S. is the single largest chip market, with Japan "just behind it and approaching [the U. S.] in size." Assuming that U. S. vendors "as a total group only have about 10% of the Japanese market," he says, the slump has to have been due largely to a drop in U. S. sales.

A source at Matsushita Electronics Corp. who asked not to be identified says projections of 1985 revenues for his firm are too low. Matsushita's sales for calendar 1984 were about $800 million, he says, and they will be about the same this year.

Matsushita's sales are flat—rather than down—this year for a number of reasons. Memory sales are a small percentage of its total revenue, although at its demand peak, it was selling 4.5 million 64-K DRAMs a month and will have 256-K samples at year end. Linear devices are still the main product and in-house sales to parent Matsushita Electric Industrial Co. are about 55% of the total. Also aiding demand are increased sales of video cassette recorders and strong TV sales.

NEC declined to make any comment on the ICE report. *–Robert J. Kozma, Eve Bennett, and J. Robert Lineback*

SEMICONDUCTORS

WHY AN OLD IC LOGIC NOW MAKES SENSE

LONDON

Britain's Ferranti Electronics Ltd. has resurrected a bipolar logic called differential current-mode logic (DCML) and is using it to build a prototype 16-bit multiplier that combines very high speed with modest power consumption.

The integrated circuit, described at the 5th International Conference on Custom and Semicustom ICs held in London last week, is a development vehicle for a family of application-specific chips based on the technology, among them a bipolar digital signal processor and a fast-Fourier-transform circuit. Ferranti also plans a family of automatically routable DCML gate arrays.

Differential logic represents a logic value as the difference between the voltages on two wires, instead of a single wire's voltage with respect to ground. Its main attraction is its ability to reject common-mode noise. Though it is not a new idea, DCML has never become popular because of the additional circuit complexity that comes with carrying signals on two lines instead of one.

But advances in computer-aided-design technology help make this added complexity invisible to the logic designer, and other improvements have helped overcome the shortcomings of differential logic, bringing its speed and power advantages to the fore. For example, modern process technology makes it possible to match many thousands of transistor pairs, load resistors, and current sources on a chip, a task differential logic makes necessary.

Furthermore, highly regular architectures with short connections between logic elements have emerged, such as the systolic array used in Ferranti's Winograd Fourier Transform chip. With such architectures, "the area penalty associated with DCML is negligible," says Stephen Colaco, manager of digital-IC design, who heads Ferranti's DCML development effort.

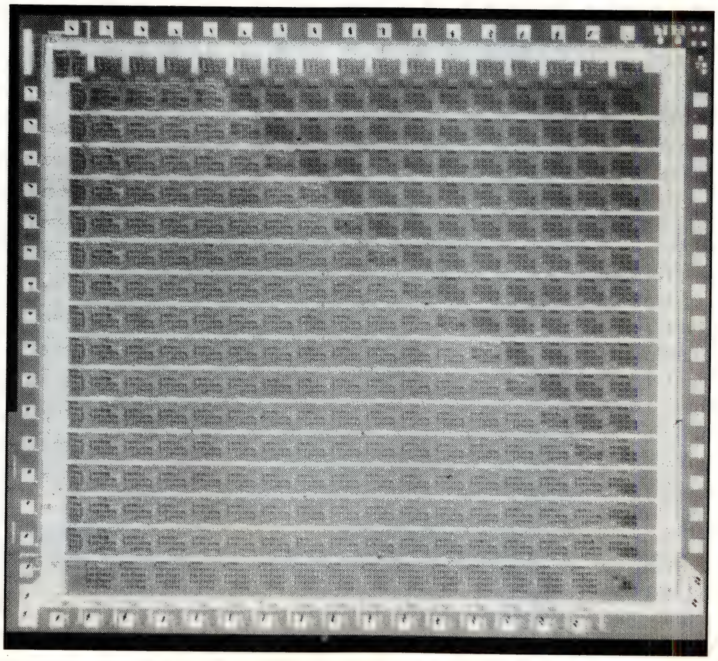
FEWER CYCLES. DCML cuts power use by an order of magnitude compared with conventional bipolar logic, says Colaco. Moreover, logic circuits designed from stacked DCML gates perform their functions in fewer cycles than equivalent single-logic-level circuits, he says, so they can be up to four times faster.

Spurious signals arising from supply-voltage and temperature fluctuations, as well as crosstalk and other noise, cancel themselves out in differential circuits. Furthermore, a differential transistor pair has a highly linear transfer characteristic. These two facts mean the logic swing can be safely reduced to 100 mV—roughly an order of magnitude smaller than the swing in conventional emitter-coupled logic. Power use shrinks in line with the voltage swing, and speed is unaffected. Also, the need to provide and route voltage references around the chip is eliminated.

The 100-mV swing allows stacking up to four levels of differential logic between the 5-V power-supply rail and ground. "Many elegant and powerful logic circuits are made possible by this," explains Colaco. These functions can be implemented with fewer gate delays in the logic. And since the logic level and its complement are always available, inverters are not needed, adds David Grundy, technical director for Ferranti Electronics.

A stacked DCML gate resembles the stacked ECL gate widely used in high-performance circuits. Both families are based on the long-tailed pair circuit. Circuits switch from one logic state to another by steering current between transistors in the long-tailed pair. This is accomplished by reversing the polarity between the bases of the transistors in each leg of the circuit.

In most ECL, a reference voltage is applied to one



QUICK MATH. A chip built by Ferranti with differential logic multiplies two 16-bit values in 25 ns and consumes only 1 W.

on-line conferences.

Such conferences are in the works. ARK, founded by San Francisco Bay-area real-estate tycoon Donald Carlson to further East-West communication, wants to establish separate on-line meetings on alcoholism, foreign trade, education, and even fusion research. Slow-scan video communication is also being established. Says Schatz, "A lot of people are beginning to realize that there is an open communications channel between East and West."

Hiltz doesn't think this particular conference will accomplish a great deal by itself, "but it may open the way for more direct cooperation between Soviet and American scientists working on problems whose solution can be of benefit to all people." *–Clifford Barney*

SPACE

SUN MAY POWER SPACE STATION'S TURBINE

CLEVELAND

There's a technology horse race going on at the National Aeronautics and Space Administration's Lewis Research Center. One contender—photovoltaic arrays—has been a mainstay of the U. S. space program for 28 years. The challenger is called solar-dynamic technology, and makes use of a concave mirror that concentrates sunlight on fluid in a receiver to heat it for driving a generator's turbine. This is an upstart technology in that it has never flown in space.

Engineers at NASA Lewis in Cleveland will choose one of the two technologies to provide power for the $8 billion U. S. space station scheduled for launch in 1993. Barring an extension, the winner will be crowned in January.

SUN POWER. NASA headquarters charged the Lewis Center about 16 months ago with the job of developing the power system for the space station—a 40-ton, permanently manned behemoth that will house laboratories, manufacturing areas, service and repair facilities, communications equipment, and other gear. Officials at the Cleveland facility have ruled out nuclear power as well as stored chemical energy sources in favor of drawing power from the sun. Now what remains is to decide is how best to do that.

One way is with silicon solar arrays, a solid-state technology that converts sunlight directly into energy without moving parts. Well understood, the technology's strengths include a proven track record in space that dates back to the first U. S. satellite, launched in 1958.

But because the space station will eventually have a power appetite about 15 times greater than any U. S. spacecraft flown to date, its solar array would have to be of an unprecedented size. The space station's initial demand for about 75 kW of average power would require a photovoltaic array of about 19,000 ft^2, or about half the size of a football field, says Daniel T. Bernatowicz, chief engineer for the NASA Lewis Power System Engineering Division. And NASA expects the station's demands eventually to grow to 300 kW.

The array's size is important because the space station will soar at about 250 nautical miles, an altitude at which drag from the earth's atmosphere will still be a factor. The more drag, the more booster fuel required on board to keep the station in orbit. That's one reason NASA sees solar-dynamic power as an attractive alternative: for the same amount of power, the drag-producing mirror area needed on a solar-dynamic system could be three to five times smaller than the necessary photovoltaic array, Bernatowicz says.

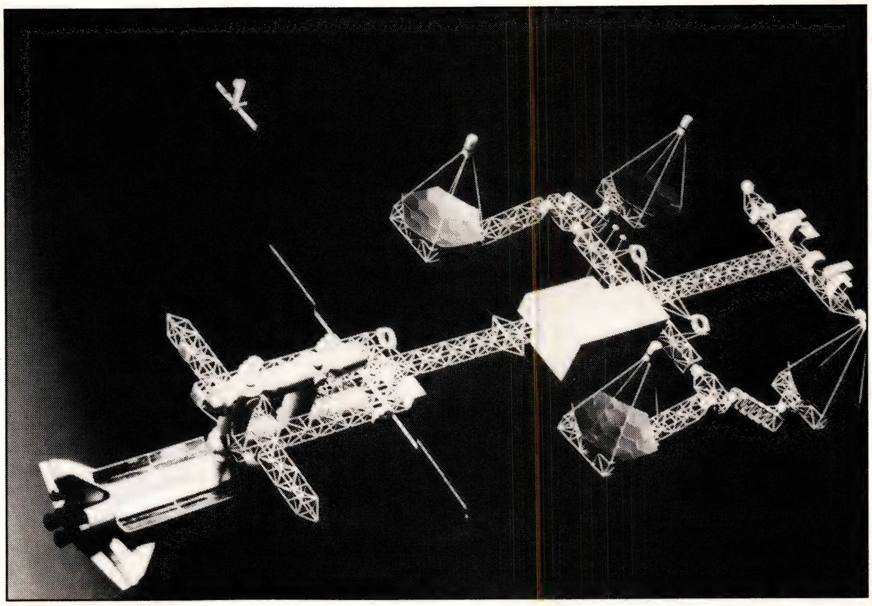
A solar-dynamic system needs to catch less light because its overall system efficiency is greater than that of a photovoltaic system. Furthermore, energy can be stored as heat in the fluid, which may be a gaseous mixture of helium and xenon, or toluene, which would pass between gaseous and liquid states. This is more efficient than the battery-storage approach used with photovoltaic systems, NASA officials say. Stored power will be needed when the space station is in darkness during 35 min of its 94-min orbit. Overall, a photovoltaic system would have an efficiency of about 10%, compared with an overall efficiency of 38% for a solar-dynamic system, says Dean W. Sheibley, chief of the NASA Lewis Photovoltaic Branch.

SOME CONCERNS. Despite the apparent advantages, however, some NASA engineers are concerned about the unproven reliability of solar-dynamic systems, which have been considered for missions in the past but never selected. Some worry that vibration from the turbine engine could interfere with some space-station experiments. The mechanical reliability of the system itself and its critical moving parts is also a concern.

NASA officials say final figures have not yet been developed for the cost of a photovoltaic array versus a solar-dynamic space-station power system. "I've seen sets of numbers both ways—that solar dynamic costs less, or that photovoltaic costs less," says Bernatowicz.

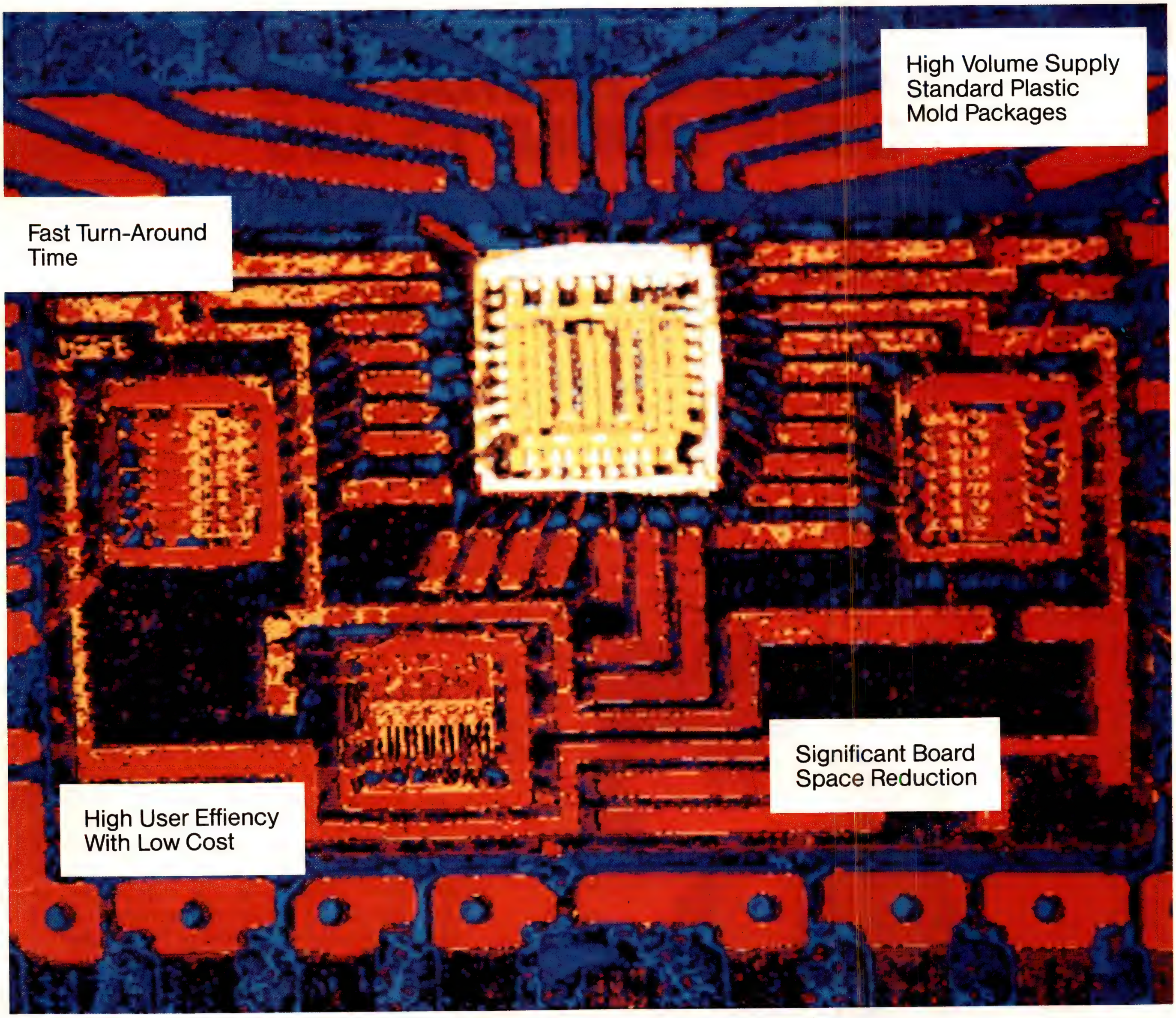
He notes that there is "heavy competition" between the Lewis Photovoltaic Systems and Solar Dynamic Systems branches as January nears. Both branches currently are developing optimum system configurations for analysis in time for the deadline, officials note. NASA Lewis is also receiving information from two prime contractors on the effort, the Rocketdyne Division of Rockwell International Corp. and TRW Inc., which have also been studying the two types of systems, Bernatowicz says.

In case a clear winner fails to emerge, NASA Lewis does have a hedge. A hybrid system using both photovoltaic and solar-dynamic systems in the space station is among those being considered, officials note. *–Wesley R. Iversen*



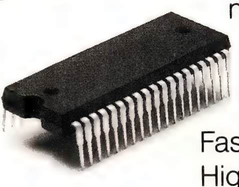
RAY CATCHERS. A proposed alternative to powering the NASA space station with photovoltaic arrays is a system that concentrates sunlight on a fluid, heating it to drive a turbine.

LSI Compact Hybrid



NEC's Semi-Custom approach to your Hybrid requirement

Our innovative fabrication process for LSI-Hybrid circuits can result in 25% board area reduction and 50% size reduction over many conventional Hybrids. NEC's new "Compact Hybrid" technology uses a PCB onto which monolithic LSI-chips are mounted together with the required active and passive components. The resulting circuit is then wire bonded and molded in a standard SIP-, DIP- or FLAT-package.



The multi-chip packaging technique used by Compact Hybrids offers:

Increased reliability
Significant user cost savings
Fast turn-around time
High volume supply by automated production
High power in small package
Significant board area reduction.

The new Hybrid concept is ideal for automative, industrial and consumer applications requiring reduced size, high reliability and large production quantities.

West Germany: Düsseldorf (0211) 650302, Telex 858996-0
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Italy: Milano (02) 6709108, Telex 315355;
Sweden: Täby (08) 7567245, Telex 13839;
UK: Motherwell (0698) 732221, Telex 777565

NEC

Circle 74 on reader service card

packages, he points out, but price competition has always forced a switch to plastic.

The production of memory devices keeps increasing, which provides an attractive market for ceramics. There is a truly rising market for ceramic PGAs, flatpacks, and chip carriers—especially the leadless variety. Leadless chip carriers also cater to the demand for smaller size, and they generate still more business for the ceramic package manufacturer because in general they must be mounted on ceramic substrates.

The continuing trends of higher pin counts and smaller equipment sizes also push the move toward PGAs, SOICs, and flatpacks (Fig. 1). PGAs retain the same 100-mil pin spacing of standard DIPs, and they can be dip-soldered. They have the disadvantage of requiring higher-priced ceramic packages, however. Except for a new package from NEC Corp., all PGA packages appear to be ceramic—but perhaps not for long. Toshiba Corp. says that it is in the final stages of testing a plastic PGA. The SOIC with 50-mil pin spacing is small, as its name suggests, but provides only a limited number of pins.

So the major trend has been toward flatpacks, says Aoyama, which have a constant size but variable pin spacing. Early units had a pin spacing of 1.0 mm, for example, but 80-pin packages have pins spaced 0.80 mm apart. For 100-pin packages, the spacing has been further reduced to 0.65 mm.

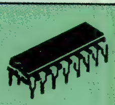
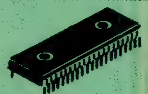
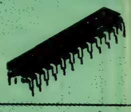
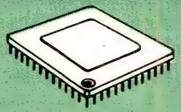
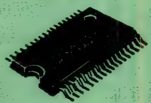
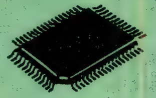
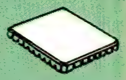
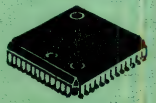
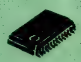
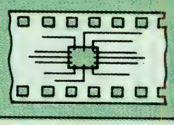
Even higher densities could be achieved by bonding multiple devices in a single package either by the chip or equipment manufacturer, says Aoyama. But he says that significant demand for such packages awaits far higher yields and reliability, or better characterization at wafer probe.

At Hitachi and Matsushita Electric Industrial Co., plastic packages predominate. Hitachi offers 256-K DRAMs in 18-pin rectangular plastic leaded chip carriers, says Gen Murakami, senior engineer in the IC Package Development Department at the company's Musashi Works. But for 1-Mb chips, he says, the package of choice will be a 20-pin SOIC with J-shaped leads for surface mounting and 26-pin body dimensions.

Hitachi's digital components started primarily as DIPs with 100-mil pin spacing, but many now come in shrink DIPs with 70-mil spacing. Other devices that were formerly packaged in 600-mil-wide DIPs are now packaged in skinny DIPs, which are only half as wide. Hitachi uses zigzag in-line packages for some linear components.

Matsushita's flatpacks use a pin spacing of 0.78 mm. A Matsushita spokesman says the trend is to use multilayer-circuit-board technology rather than higher-cost ceramic packaging for PGAs. But the problem of large size remains.

THE WIDE RANGE OF JAPANESE IC-PACKAGES

Type	Package		Lead pitch
DIP		🔵 🔴	• 2.54 mm (100 mil)
Shrink-DIP		🔵	• 1.778 mm (70 mil)
Skinny-DIP		🔵	• 2.54 mm • Width ½ size
Zigzag in-line		🔵	• 2.54 mm • Two rows
Pin grid array		🔴	• 2.54 mm (100 mil)
Small-outline		🔵	• 1.27 mm (50 mil) • Leads on two sides
Flatpack		🔵	• 1.0 mm • 0.8 mm • 0.65 mm • Leads on four sides
Leadless chip carrier		🔴	• 1.27 mm (50 mil) • 1.00 mm (40 mil) • 0.75 mm (30 mil)
Leaded chip carrier		🔵	• 1.27 mm (50 mil) • J-leaded
Small-outline J-leaded		🔵	• 1.27 mm (50 mil) • Two rows
Tape automated bonding		🔵	• Thin package

🔵 Plastic 🔴 Ceramic

THE MOVE TO TAB

NEC Corp. claims to be the only company selling standard gate arrays in plastic pin grid arrays. PGAs with 72 and 132 pins are now available, and a 208-pin package will appear by the end of the year. Plastic PGAs cost about 30% more than flatpacks, but are still cheaper than their ceramic counterparts, which cost about twice as much as flatpacks. The packages hold two separate series of CMOS gate arrays with internal gate propagation delays of 2.0 and 1.4 ns in sizes up to 20,000 gates.

Hitachi's Murakami says the demands for smaller packages will dictate the move from flatpacks to TAB. Chip-on-board suffers from the same problems as multiple chip packages and appears to be used mainly for special applications, including watches and program cartridges for personal computers. It is sometimes used to squeeze a chip or two onto a small subassembly board with surface-mounted devices, but it is avoided when possible.

Hiroaki Fujimoto of Matsushita's Advanced Device Laboratory agrees that TAB will increase in the future. He says wire bonding is cheaper for 60-lead chips; but as the number of leads exceeds 100, TAB becomes cheaper and faster—and clearly smaller. Even so, Matsushita is using a 64-lead TAB for a thermal-head driver because the 0.12-mm pitch required is finer than is possible with wire bonding. Similar technology is also appropriate for display drivers.

One problem with TAB is the need for bumped chips, which requires additional IC processing. Matsushita has developed a process that makes it possible to use regular chips by bumping the leads of the pattern on tape (Fig. 2). Matsushita can then bond only the electrically good chips, and no chip price premium is incurred. For assembly manufacturers, this also solves the problem of chip makers' unwillingness to bump chips for them. U. S. producers of tape on the functional IC's flexible substrate to pads on the board. Functional ICs are available for the color processing, luminance processing, and audio FM circuits common to many VCRs.

Sony Corp. uses varied fabrication techniques for its products. For 8-mm camcorder signal circuits, Sony attaches flatpacks on the back of the board with adhesive. For the top, cream solder and infrared reflow are used. Sony uses a laser system on large boards with only one or two flatpacks to eliminate heating produced by reflow soldering. The problem, though, is amortizing the cost of the laser-soldering system.

Sony relies on a mix of modules and functional ICs because the same circuits are needed in many products, and there is economy of scale in the modules. Hybrid-like modules account for about 10% of its total linear ICs, but only about 25% of them are true hybrids. Some modules are combinations of pc-board and hybrid IC techniques.

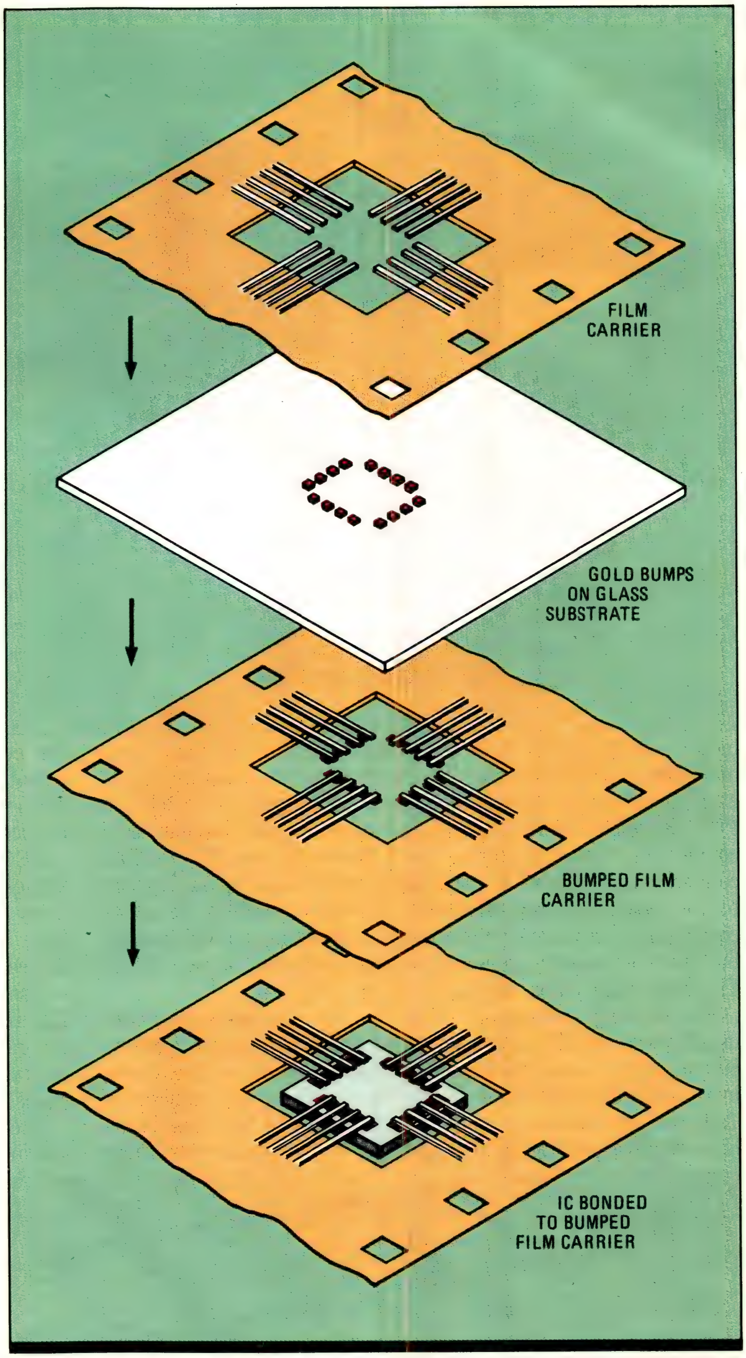
A camera video signal IC made with thick-film technology on ceramic, for example, incorporates two wire-bonded signal ICs, an SOIC, and Minimold transistors soldered in place. A video part on ceramic has about 80 components, including a flatpack IC, in an area about 25 by 25 mm. Sony uses a vapor-phase system to reflow-solder both sides at once.

Some of the modules hold polymer thick-film resistors that are printed directly on glass-epoxy printed-circuit boards. The resistors' accuracy of initial value and drift are not so good as for the same type printed on ceramic substrates, but they are adequate for many products.

LOTS OF LAYERS

Japanese computer packagers are just as clever when it comes to high-density high-speed systems. A remarkable example of surface mounting in professional equipment is Hitachi's M-68X computer, in which 419-by-280-mm logic boards hold 72 LSI flatpacks—either bipolar gate arrays or memory modules (Fig. 4). The polyimide-glass boards have a total of 20 layers of interconnections: two surface layers, eight signal layers, and 10 power and ground layers.

Perhaps most remarkable is the design of the surface layers, says Fumiyuki Kobayashi, senior computer-development engineer at Hitachi's Kanagawa Works in Hadano City. Kobayashi says the design makes it possible to cut pc-board traces and add jumpers should field changes be necessary. Despite the large scale, the boards are a product of extreme precision—through-hole pitch is a mere 50 mils. Traces on the board have a center-to-center pitch of 10 mils (actual trace width is 4 mils, spacing is 6 mils).



2. BUMPED-TAB. A bumped film-carrier tape allows the use of standard chips in tape automated bonding. Matsushita's method transfers gold bumps on a glass substrate to the inner leads of a tape pattern.

Each board typically has 100,000 gates, which necessitates a large number of input/output connections. There are four main connectors with four groups of 260 pins each to plug into the motherboard. There are also eight cable connectors with two rows of 48 pins—a total of 768, of which 448 are signal pins. The connector pins are pitched at a tight 50 mils.

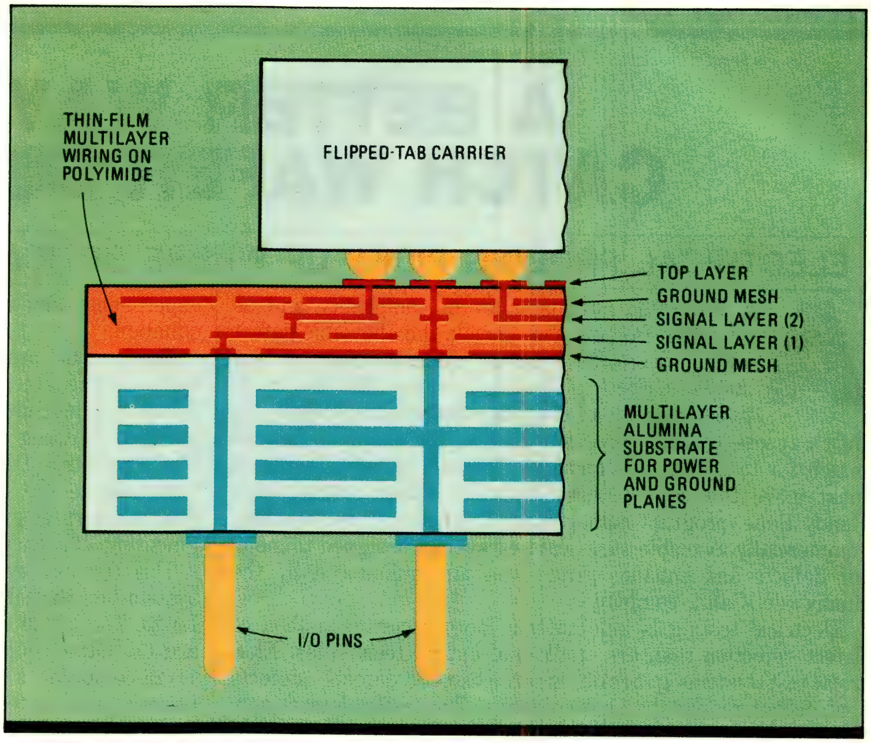
Hitachi houses the 2,000- and 5,000-gate arrays in 22-mm^2 ceramic flatpacks. These are emitter-coupled-logic chips and have 160 leads—40 on each side—with a pitch of only 20 mils. Hitachi chose flatpacks rather than the more standard 100-mil-pitched PGAs for smaller size.

Cache-memory modules are in 29-by-39-mm ceramic flatpacks with two rows of 48 leads pitched at 30 mils. Modules have eight ECL SRAMs on one side and one LSI chip on the reverse. Chips are either 16-K types with 12-ns access times or 4-K types with 4.5-ns access times. Also on the board are groups of 32 thick-film terminating resistors in flatpacks with 40 pins, 20 on a side, with 20-mil pin pitch. Two resistor packs can be used at each LSI-chip position.

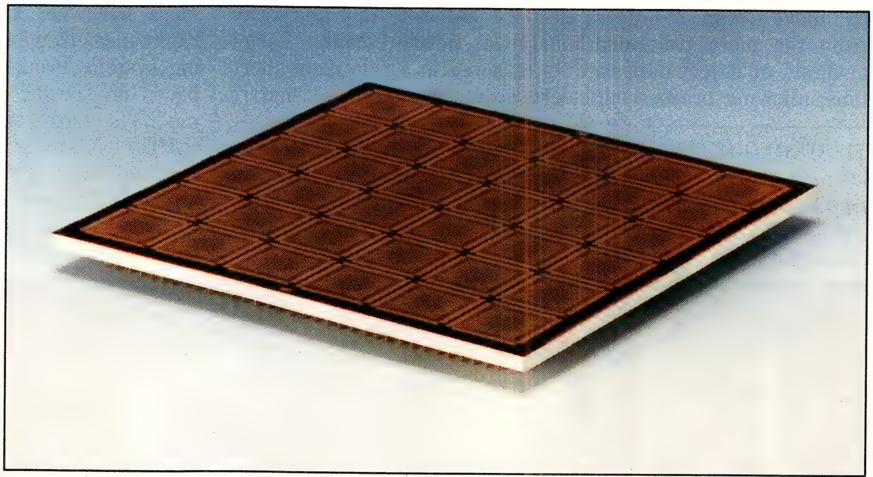
The total number of pins on these boards approaches 20,000. Laser reflow soldering using proprietary equipment makes the connections—all of which must be good. Both electrical and visual checks of these boards are performed for quality assurance.

Hitachi's supercomputers use an earlier version of the same type of board, with control logic on the front and vector registers mounted on the back for almost zero propagation delay in the connections between these two functions.

For I/O, Hitachi uses the same size board but more conventional fabrication techniques to attain the very high density of eight channels per board. Each channel has its own controller inserted in zero-insertion-force sockets and studs from liquid-cooling modules contacting individual flipped-TAB carriers for efficient heat removal.


THIN-FILM MULTILAYER WIRING ON POLYIMIDE
FLIPPED-TAB CARRIER
TOP LAYER
GROUND MESH
SIGNAL LAYER (2)
SIGNAL LAYER (1)
GROUND MESH
MULTILAYER ALUMINA SUBSTRATE FOR POWER AND GROUND PLANES
I/O PINS

5. SUPER SUBSTRATE. The NEC supercomputer has a multilayer structure for mounting arrays of tape-automated-bonded chips. The substrate (below), a composite of ceramic and polyimide, has 12 power planes in the ceramic and five wiring levels in the polyimide.



Hybrid technology is widely used in Japan. Recent estimates from the Electronic Industry Association of Japan place the merchant market at about 100 billion yen, or $470 million. If the captive hybrid output is taken into account, the total value hits about 300 billion yen. Unlike their U. S. counterparts, Japanese hybrids are practically all consumer types, and most are soldered rather than wire-bonded. Major Japanese markets for hybrids are in VCRs, color TVs, and in automobile electronic modules for thick-film circuits and telecommunications and thermal printheads for thin-film circuits.

Toshiba uses its hybrids for a wide range of applications. Many leaders in hybrid fabrication, on the other hand, owe their large volume to concentrating on a narrow range of products. Hitachi and NEC, for example, use hybrids mainly in their large computers. Tokyo Sanyo Electric Co. uses a patented process featuring an aluminite insulating film on aluminum to build power amplifiers, and Sanken Electric Co. concentrates on power-amp and power-supply series regulator modules.

One type of hybrid popular at Toshiba is the multichip-on-ceramic type, which Kyocera Corp. characterizes as hampered by chip yield and reliability problems. Toshiba sets up its lines on the assumption that rework will be needed. Initial yield after wire bonding is typically on the order of 70% to 80%. But extensive rework is not usually required—yield after changing one chip is more than 95%, and it is uncommon to have to change more than two chips.

Toshiba uses these hybrids for a variety of applications, including read-only-memory and RAM modules, circuit modules for medical equipment, in communications equipment, and even as logic and drive circuits built into the thermal heads that print tickets in subway and railway vending machines.

Hermetically sealed inert gas provides higher reliability than plastic-encapsulated packages, and compact configuration provides better performance. The thermal heads with serial-to-parallel conversion and drivers built into the same package permit a head with hundreds of elements to be driven by about 10 external connections. Chip count in early thermal heads neared 20, but the latest design requires only 11 chips. Manufacturers tend to redesign these hybrids every two or three years because higher-density ICs keep appearing.

FABRICATING COMPONENTS ON BOARD

More innovative are methods that use laser beams to fabricate resistors and conductors on pc boards. These techniques could be especially suited to producing low production runs of custom boards with a computer-aided-design and -manufacturing driven system.

Resistor fabrication involves the application of a resin paste on a resin pc board and then carbonizing the cured paste with a laser of the type usually used for trimming resistors. The resistance value can be monitored during the process to set it close to design value. Researchers have used this technology in a headphone stereo system to experimentally fabricate 36 resistors, with values ranging from 47 Ω to 390 kΩ.

A conductor-fabrication method is even newer and has not been tested extensively yet. Starting material is an organic resin containing dispersed copper particles. During conductor fabrication, a portion of the resin undergoes thermal decomposition and the copper particles are brazed to form a conductive line about 0.12 to 0.14 mm wide. Resistivity of the lines is lower than that of silver-palladium thick-film pastes normally used for hybrid circuits.

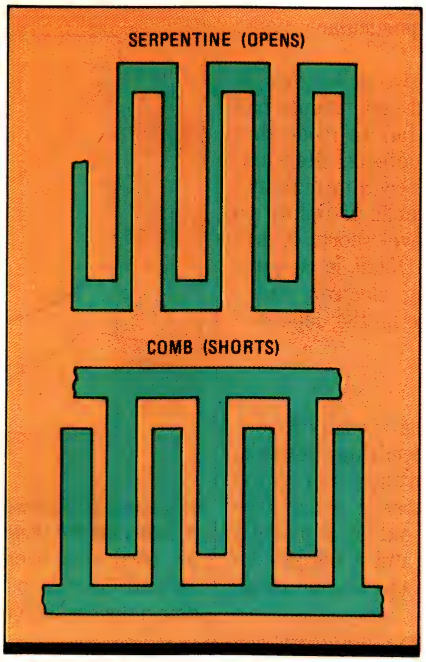
Toshiba makes commercial solid-state relays on a 0.150-mm resin film insulator applied to an aluminum substrate, which offers good heat conductivity. Laser trimming improves the precision of the thick-film resistors. In addition, copper-paste resistors are nickel plated and solder coated for lower resistance and improved reliability. An experimental watt-hour meter fabricated on an enameled steel sheet forms part of the unit's case. □

ing major yield-loss mechanisms.

The new system features work-site data-management capability that significantly reduces the intensive labor associated with defect reduction. Process engineers interact with the Lithomap's computer system, interpreting and analyzing the data output. The system stores up to 1,000 data sets of defect data, which can be retrieved or analyzed easily. Report-formatted outputs such as statistical tables, wafer maps, histograms, and, in particular, graphical expressions of yield models significantly reduce the effort of sustaining a comprehensive defect-reduction program.

The DM20 defect-measurement option works by detecting process-induced failures in electrical test structures. These structures are patterned onto a thin film, forming an array of conductive lines and spaces on test wafers. The electrical integrity of each structure is determined by probing for shorts, opens, and leakage.

The prober takes about 20 minutes to test 240 test structures patterned onto each wafer. Defects are detected when the parametric values measured during the test lie outside the acceptable limits and meet a failure criterion.



2. SHORTS AND OPENS. Wafer test structures consist of combs, which are sensitive to shorts, and interdigitated serpentine patterns, which detect opens in the pattern.

The degree to which the system can correctly assess defect density depends on the quality of the information obtained from the test structures. Test-structure design, layout, test conditions, and pass/fail criteria are of particular importance. In addition to its products, Prometrix provides the expertise that is necessary to ensure a successful defect-reduction program.

A major cause of defects is process equipment, Bane points out. In fact, early tests with the DM20 on a customer's test wafers indicated that a particular piece of process equipment was the main defect contributor because the equipment introduced particulate contamination during processing.

THE BIG CLEANUP

Historically, IC manufacturers were left to remove contaminating particulates from process equipment after use. Processing engineers want to change that by enforcing stricter defect-density specifications on process equipment. To that end, the equipment must meet and maintain defect-density specifications that are lower than those that used to be acceptable.

Currently, most suppliers of IC-processing equipment do not supply defect specifications on their equipment, and no standards for defect measurement exist. Clearly, this will not be acceptable for future very large-scale-integration devices; a machine such as the DM20, which accurately measures defect density associated with fabrication equipment, will be a required analytical instrument for both IC manufacturer and process-equipment vendor.

Defects generally show up as either opens or shorts in the patterned film. A combination comb and interdigitated serpentine, or meander, thin-film pattern on the test wafer is used to sense the two types of defects. The combs (Fig. 2) are sensitive to shorts, and the serpentine detects opens or breaks in the conductive pattern.

An assortment of optical targets is also placed on the test chip to facilitate postelectrical optical inspection. This optical inspection can help determine the exact origin of a defect.

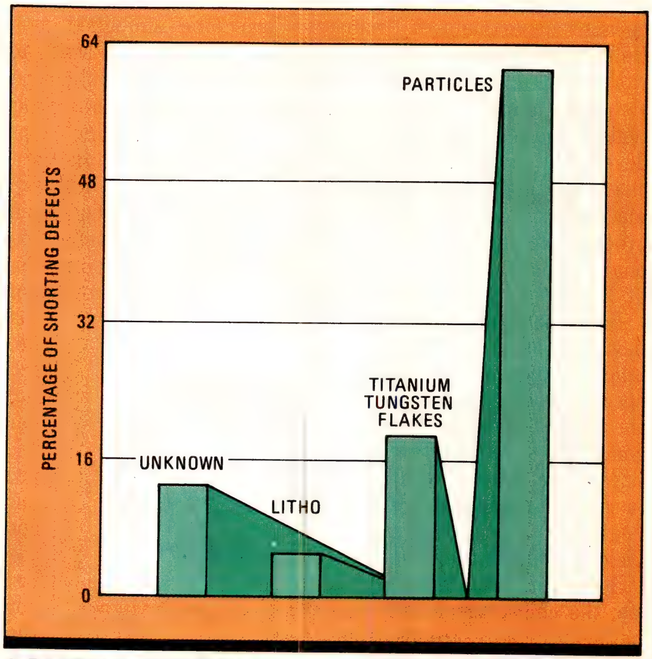
Test structures can be designed to be sensitive to other types of process-induced failures. Additional failure mechanisms that these electrical test structures can monitor are junction leakage or pipes, open contact strings, and leakage through dielectric layers. By establishing a relationship between test-structure yield and product yield, a comprehensive yield budget can be developed.

A proper budget establishes the defect density required to achieve a specific die-yield goal. Each critical process step's defect density is measured, and a reduction goal is assigned. The DM20 helps the process engineer achieve this defect reduction by providing a complete environment to gather and analyze split-run experiments efficiently. This characteristic of the system permits the engineer to concentrate on fixing the defect.

Achieving a good correlation between test-structure yield and product yield requires that test wafers be generated at each process module or masking step. The structures must also be sensitive to most of the product-failure mechanisms.

Prometrix believes that a successful yield-improvement methodology can be maintained by targeting these modules in terms of defect density versus a particular piece of equipment, or in terms of a slightly different process, different feature sizes, load position, cleaning frequency for the process equipment, and overall defect density over time.

The Prometrix LM20 defect system permits chip producers to collect and interpret enormous amounts of test-structure yield data quickly. Judicious use of this information will permit IC manufacturers to improve the profit margins on their chips by increasing die yields. Yield models can be used in a production mode in order to detect excursions from the norm by monitoring the defect density over time for a particular



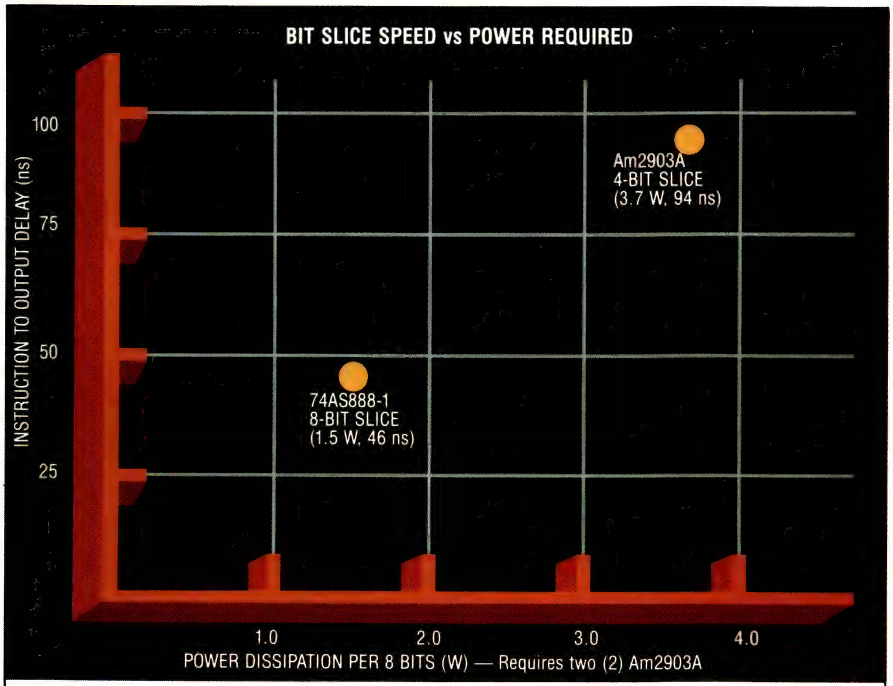
3. PARTICLE PERCENTAGE. In a breakdown of defect sources (shorts) in a three-level metal structure placed over thermal oxide, the percentage of lithography defects turns out to be small. Contaminant particles introduced by processing predominate.

Design for faster system performance with new IMPACT 8-bit-slice processor from Texas Instruments.

- **Outstanding speed,** low power, and flexibility of TI's advanced 74AS888 processor boost system throughput (*page* 2).
- **Cost-effective digital control** is provided by TI's single-chip, high-speed TMS32010 signal processor (*page* 3).
- **Dramatic savings in system power** are achieved using TI's new CMOS THCT1010 multiplier/accumulator (*page* 4).

▶

delivers 51% greater throughput.



Impressive speed/power performance is possible by using TI's new 74AS888 processors. 0.8-ns internal-gate switching and 100-μW internal-gate power dissipation contribute to the 51% speed improvement of the 74AS888-1 as measured by instruction-to-output delay. Power is reduced by 60%. The unique IMPACT (Implanted Advanced Composed Technology) process developed by TI is used to fabricate the 74AS888 processors. IMPACT techniques include oxide isolation and composed reticles to achieve 2-micron geometries essential to the development of advanced VLSI products.

Flexible instructions for complex math

Fixed instruction sets limit the kind of operations a microprocessor can be programmed to do. But you program the 74AS888 using a comprehensive set of microinstructions — 13 arithmetic and logic functions, 8 single- and double-length conditional shifts for magnitude scaling, and a wide range of bit-, byte-, and word-manipulation instructions. With TI's 74AS888 you can tailor an instruction set precisely to your application. Use any software. Use any word length in 8-bit increments. Even emulate any known μP instruction set, achieving substantial improvements in system throughput.

High-speed 74AS890 microcontroller supports symmetrical pipelining

Microcoded instructions are stored separately from main memory, generally in a high-speed PROM or static RAM. Handling the sequencing and batching operations between this storage space and the 74AS888 is TI's high-speed 74AS890. It is a 14-bit microinstruction controller that can address up to 16K of control-store memory. The 74AS890 can also serve as a powerful, stand-alone sequential controller.

The 74AS890 can perform 16-way branch operations, realtime interrupts, and nondestructive reads of a nine-word-deep stack. Two 14-bit counters can be used for nested-loop operations. The maximum clock-to-output delay of 42 ns for the 74AS890-1 balances the memory microcycle timing with the 74AS888-1 data-execution timing cycle.

Space-saving, economical packages

Now available from TI distributors in a 68-pin ceramic grid array, the 74AS888 and 74AS890 will soon be available in a 68-pin plastic leaded chip carrier. Both packages are offered at the same price. Military versions will be available in leadless ceramic chip carriers.

The price of the 74AS888-1 is $166.00 and that for the 74AS890-1 is $87.00, in 100-piece quantities each. The price will decrease according to high-volume purchase commitments.

TI's single-chip DSPs with 200-ns cycle time: Low-cost solution to high-speed control.

An extremely effective alternative for improving system performance is TI's TMS32010 Digital Signal Processor, which can be applied in high-speed-controller applications where digital control replaces analog servo-loop processing. Having a high degree of integration and an outstanding combination of features, the TMS32010 is very cost-effective (1) as an application-specific controller in existing bit-slice designs or (2) as a stand-alone controller handling the multiple functions often required by a single application.

For example, the TMS32010 could enable an industrial robot to perform mechanical operations through digital/servo-loop computations, to synthesize and recognize speech, and to sense objects with radar or optical intelligence.

Having a 200-ns instruction cycle, the TMS32010 gives you the flexibility of a high-speed controller and the numerical capability of an array processor in a single 40-pin DIP. The TMS32010 contains on-chip data RAM, on-chip program ROM, a 32-bit ALU/accumulator, a 16 × 16-bit parallel multiplier, and a barrel shifter.

Seven TMS32010 Application Notes, including one entitled *Control System Compensation and Implementation,* are available. For the set, send us the coupon from page 4. ■

Extensive support

Third-party development support is in place and ready to help you with your implementation of 74AS888 bit-slice systems designs.

If you have questions, a call to **(214) 995-4720** puts you in touch with TI's applications support group. Your nearest TI Regional Technology Center can also answer your questions and tell you about future 74AS888 training courses.

For more information on the 74AS888 and 74AS890, clip and complete the coupon on page 4. ■

Turn page for more information.

70-BIT PROCESSOR CHIP WILL DO COMPLEX DECISION MAKING

THOMSON-CSF TAKES NEW TACK TO MANAGE HUGE VIRTUAL MEMORY

Computer-aided decision making is coming fast. Many new applications will rely on this tool—everything from artificial intelligence and expert-systems to computer-aided design and military command and control—and it will require large numbers of stored information models rather than computed ones. Consequently, the next generation of computers will need sophisticated memory-addressing capabilities to ensure data consistency and protection for large quantities of valuable and confidential data. This could require a computer with a radically different design.

At least executives at France's giant Thomson-CSF conglomerate think so. They say the computer industry will have to abandon standard-architecture microprocessors and find a different solution by the early 1990s, the time when they expect such applications to begin showing up. Because of this scenario, Thomson is hard at work on one new solution, a project that the company has codenamed SCQM [*Electronics*, Nov. 4, 1985, p. 20].

SCQM's goal is to develop an object-oriented and capability-based processor that can access a large distributed virtual-memory space. This space is made up of objects, each identified by a unique name—48 bits of a 70-bit virtual address. Data, in the form of 4-byte-wide words, is accessed with these 70-bit addresses, which result from the concatenation of the 48-bit object name and a 22-bit offset address within the object.

"The virtual addresses are more like a social security number than an address for a given set of data. Once one is assigned, it is never reused," says Jacques Leroudier, the project's team leader. The 48-bit names are large enough to create new names at a high rate for many years; objects, once created, can retain their unique name for the life of the system.

The virtual-memory space provides the computer user with a single-level memory scheme that hides the usual memory hierarchy of main-memory and mass-storage devices. Such schemes replace both memory-management and file-storage systems of standard computers.

The objects are like the drawers of a filing cabinet, where each drawer is strictly classified and individually locked. When creating an object, a user of the SCQM system is simultaneously creating an unforgeable key that holds the unique object name. Such a key is usually referred to as a capability.

The owner can duplicate the key to give it to other users, either as a whole or with certain access rights withheld. Any user who has a copy of the key can access the object and carry out operations that correspond to the access rights assigned to his or her version of the key. So the use of an object is dependent upon having the necessary key endowed with the appropriate access rights.

SCQM objects are coherent by function. If, for example, an object is designated as a mailbox, it is impossible to use it to do mathematical calculations.

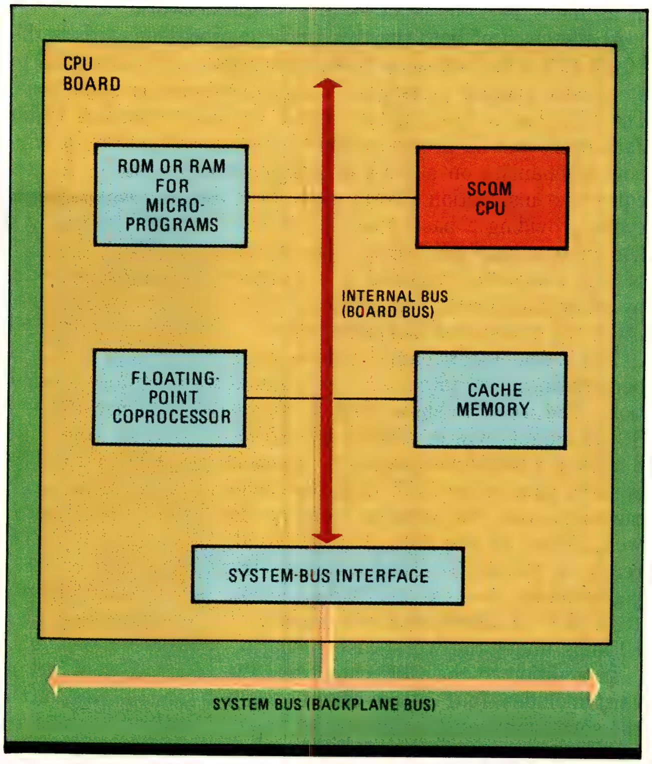
Power is furnished by a reduced-instruction-set-computer (RISC) central processing unit (Fig. 1). Thomson is developing six other chips to support the CPU: a cache-memory module chip, a main-memory controller chip, and a system-bus-interface that includes four chips—a cache directory, a bus arbiter, a bus monitor, and a controller.

The prototype versions of these seven chips are being made in a 1.2-μm CMOS technology with three interconnection levels (one polysilicon, two metal) and a propagation delay of 0.5 ns. The chips are designed to dissipate a maximum of 3 W each and feature a packing density of 1 million transistors per square centimeter. They will be mounted in packages with up to 256 pins. In an effort to optimize performance, the production versions will be made with 0.8-μm technology to keep chip sizes to a maximum of 50 mm^2.

CLUSTERED ARCHITECTURE

The overall SCQM architecture is composed of clusters consisting of at least one CPU card, an input/output processor card, and a number of memory modules all connected to the SCQM system bus (Fig. 2). A peripheral bus connects peripherals to the I/O processor cards and provides the gateway to the intercluster communication network. In Thomson's prototype, the peripheral-bus function will be executed by a VMEbus. Because the peripheral bus connects to the SCQM by way of an adapter, other standards, such as Multibus II or Futurebus, can be substituted easily.

A cluster can be a multiprocessor containing up to 16 CPUs. Distributed systems can be built by interconnecting the clusters through a network. Accessing information from anywhere within an SCQM network is completely transparent for the user because the same 70-bit virtual object ad-


CPU BOARD
ROM OR RAM FOR MICRO-PROGRAMS
SCQM CPU
INTERNAL BUS (BOARD BUS)
FLOATING-POINT COPROCESSOR
CACHE MEMORY
SYSTEM-BUS INTERFACE
SYSTEM BUS (BACKPLANE BUS)

1. ALL ABOARD. The CPU board of Thomson-CSF's SCQM architecture contains the 70-bit SCQM microprocessor chip, microcode memory, cache memory, and an optional floating-point coprocessor.

THE DRIVE TO HEAD OFF A CRISIS IN TEST SOFTWARE

FOCUS IS ON STANDARDS, AUTOMATED GENERATION, OFF-LINE DEBUGGING

by Alexander Wolfe

Manufacturers of automated test equipment face a software crisis—they are struggling to keep up with the demand for the programs needed to test today's complex very large-scale integrated circuits. As the testing job gets tougher, the software takes longer to develop. That's why speeding up the software development cycle is the only way to effectively stave off this predicament.

So ATE makers have launched a multifaceted drive to improve productivity in writing software. They realize they are pursuing a moving target, as complete systems on a chip, which are becoming available as the Department of Defense's Very High-Speed Integrated Circuits program moves forward, will only increase the gap between test performance and need.

ATE makers and users will reap important savings from increased productivity. Test systems for today's dense VLSI chips not only involve a substantial capital outlay, but the cost of programming and maintaining such a system over its useful lifetime adds up fast. According to Teradyne Inc., an automated-test-equipment manufacturer, the total can easily run 3 to 10 times the initial purchase price.

Makers of ATE are focusing on the software problem by adopting three approaches: test-software standards, automated generation of software, and an integrated approach to developing test software. All three will come into focus next week at the International Test Conference in Philadelphia.

One suggested solution to the crisis comes from Hewlett-Packard Co. in its call for a common language for the interchange of test data. Until now, it has been difficult to tie together the data from disparate machines without a lot of custom software to handle the machines' differences. "There hasn't been a common way that anybody could create data from testers of all different kinds of manufacturers and get data into data bases that can do analysis," says Reed I. White, manager of HP's TC-10 tester data-collection project.

To solve this problem, HP has developed the Data Transport Standard. "What we've attempted to do is come up with a standardized means for moving data so that any application can create data [and] any other application can interpret it," says White. The Data Transport Standard could be the first attempt at such standardization, he says.

To date, the Data Transport Standard has been offered only informally. The test conference paper will mark the language's public introduction. As a language for transmitting data between pieces of test equipment, it is unlike standard computer-programming languages. Standard languages are geared to listing instructions, whereas data languages are optimized for representing data. Because the Data Transport Standard is geared for communicating data between different machines, it is formulated as a general-purpose data language.

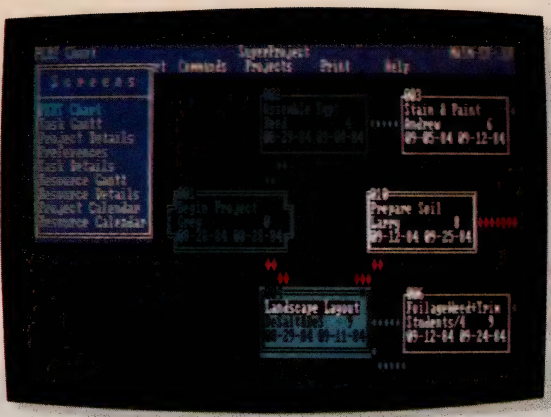
The Data Transport Standard was implemented through a two-level scheme that was designed to make it compatible with the International Organization for Standardization's seven-layer model for open-systems interconnection. It corresponds to the sixth layer of the interconnection model.

Higher up, at OSI layer 7, is the Test Result Standard. This standard, which accompanies the Data Transport Standard, nails down the specifics of how the records will actually travel between computers, including how the records should be sequenced and what the various fields should contain. Test Result Standard software is designed to handle communications problems such as link failure and program aborts without damaging the data. The Test Result and Data Transport standards can work with any type of hardware bus or data-communications link, notes White.

In the Data Transport Standard, words are transmitted in groups, known as data-transport records. These are variable-length flexible records consisting of a header that identifies message type, and a number of data words. Data is sent in bundles of up to 2,000 bytes. The records can be converted to a number of different styles as needed—binary or ASCII, for example—for use on different types of equipment.

The Test Result Standard also defines records for carrying the kind of information contained in wafer maps used during the semiconductor-fabrication process. (Semiconductor manufacturers would constitute a large market for equipment us-

MIX AND MATCH. Standard software would permit a mix of systems.



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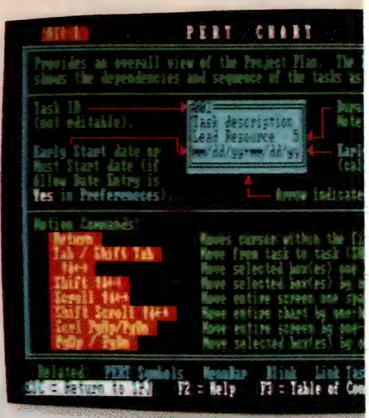

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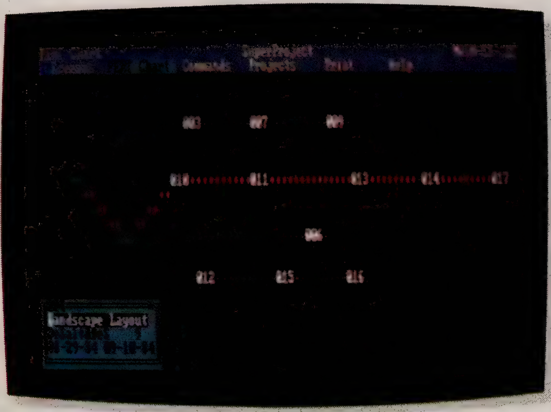

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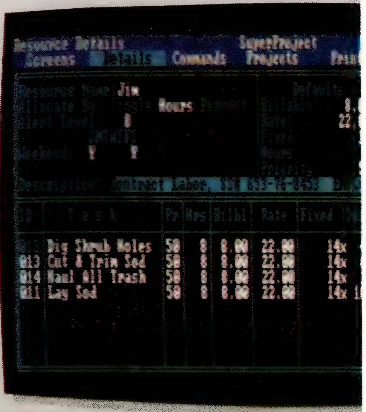

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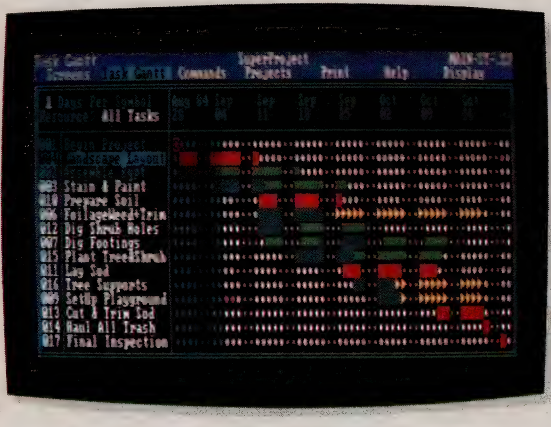

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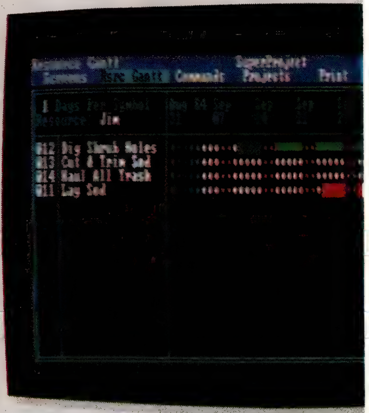

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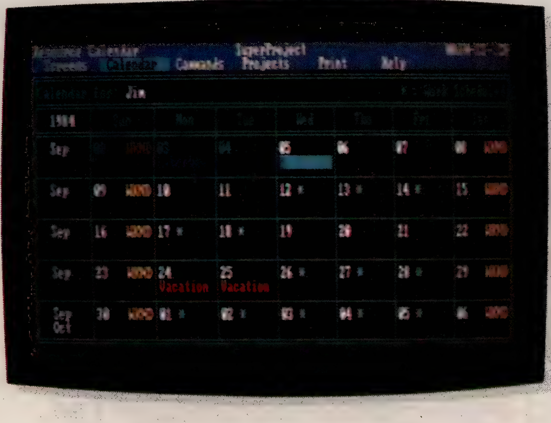

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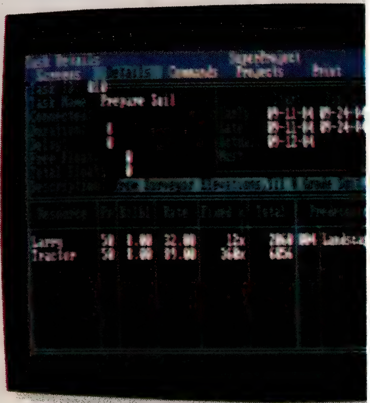

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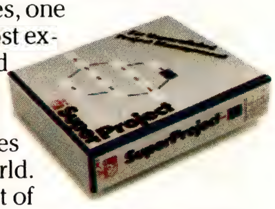

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Circle 43 on reader service card

PROBING THE NEWS

WHY THE JAPANESE ARE PARING CHIP-MAKING PLANS IN THE U. S.

DISAPPEARING PROFITS SLOW AMERICAN EXPANSION

by Michael Berger

TOKYO

The "American strategy" that Japanese semiconductor makers adopted to blunt U. S. protectionist sentiment is in trouble. Originally, the Japanese planned to shift up to 50% of their total production to subsidiary plants in the U. S. But when the American semiconductor market took a nose dive, Japanese chip makers started revising downward their game plans.

With the chip market still not signaling any strong upturn, especially in the Japanese-dominated memory business, the Japanese chip companies are scaling back or delaying their expansion of U. S. facilities. Some industry observers think this is a short-sighted strategy that could ultimately backfire, just as it did for U. S. companies in the late 1970s. U. S. chip vendors are doing the same thing in Japan: plans to build chip plants are on hold.

Sales of Japanese semiconductors in the U. S. market, which totaled more than $1.8 billion last year ($1.5 billion in exports, $333 million in sales by U. S. subsidiaries), will probably be down by an average of 30% in 1985, predict Japanese semiconductor executives. "We're suffering even more than the Americans because Japanese makers are so heavily involved in the memory market," claims NEC Corp. senior vice president and director Tomihiro Matsumura.

PLUMMETING PRICES. NEC, he says, is not as exposed as its rivals—about 32% of NEC's total semiconductor output is in memory, versus close to 45% for Fujitsu Ltd. and Hitachi Ltd., Matsumura says. Even so, NEC's chip sales, like those of all other major Japanese makers, will decline in 1985 from 1984. The Japanese control more than a 90% share of the world market for 256-K dynamic random-access memories, but that's 90% of a disaster, say analysts. The average price of a 256-K DRAM was $13.79 in Japan last year; this month, it's $1.53, and heading lower.

The dilemma for the Japanese is that while the market slump continues, pressures from the U. S. to invest further in U. S. production are increasing because of the trade deficit. NEC is even thinking about importing its U. S.-made chips to reduce its "in-company" trade imbalance, says Matsumura. But he admits this strategy does not address the broader problem: how to cope with the effects of a changing industry in which their increased market share makes Jap-

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FAULT TOLERANCE BEGINS TO LURCH INTO THE MAINSTREAM

BUT ONLY TWO PLAYERS ARE BRINGING PRODUCTS TO MARKET

by Craig D. Rose

BOSTON

The demand for less downtime in nearly all applications is moving fault tolerance from niche status to the mainstream. Yet despite the likelihood that demand for fault tolerance will become nearly universal, most large computer companies have not entered the market for fault-tolerant systems, and many smaller ones have had rough going in pursuit of it.

At present, just two companies share nearly the entire fault-tolerant-systems market (chart). But the competition will soon diversify. Perhaps most important, IBM Corp. has launched full-scale marketing efforts for a fault-tolerant system, albeit one made by another company. Several smaller companies are finally ready to move long-delayed products out the door. At the same time, market forces are prodding companies offering fault-tolerant features into new areas.

Fault-tolerant machines, which can keep running even when major components crash, promise extremely high availability by ensuring that downtime is rare. The two different approaches to fault tolerance are exemplified in the machines from the industry leaders. Tandem Computers Inc.'s units use complex system software to shift functions and data among hardware elements, whereas those from Stratus Computer Inc. rely strictly on duplicated hardware.

The new lure for entering the business, which to this point has consisted largely of sales to brokerage and financial institutions, is the expectation that fault tolerance will find broad new applications, particularly in computer-integrated manufacturing. The thinking is that as computers assume more vital roles, the need to minimize downtime to control costs will become crucial.

CIM is particularly appealing for two reasons. One is that downtime on production lines can cost many thousands of dollars. The other is that the growing acceptance of General Motors Corp.'s Manufacturing Automation Protocol (MAP) factory-automation standards [*Electronics*, Nov. 4, 1985, p. 55] could accelerate implementation of integrated factory systems. The CIM market, which has no established leaders, is also more accessible to the newer makers of fault-tolerant computers.

CHANGE. Stratus president Foster eyes the computer-integrated-manufacturing market.

To succeed in CIM, fault-tolerant-computer makers must increase the emphasis on networking and communications, says Gerald Held, director of strategic planning at Tandem, Cupertino, Calif. In addition, the ability to size systems and expand them over a broad range is a big plus on the factory floor. Tandem believes the expandability of its systems will help it crack this market.

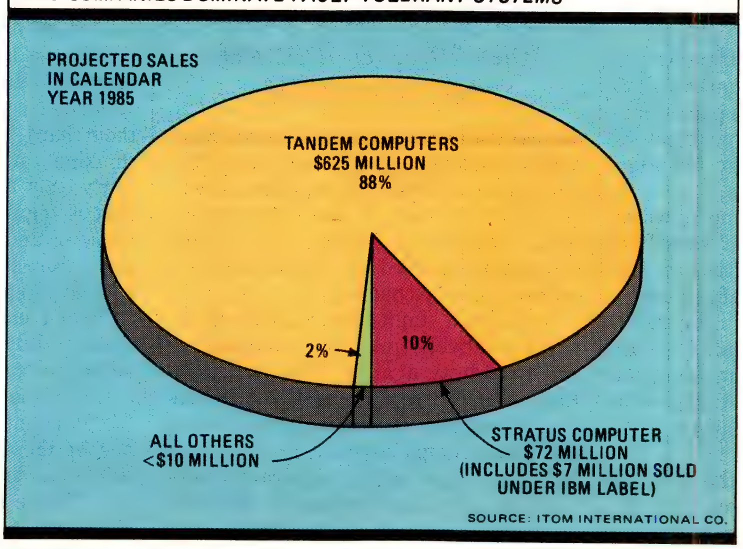
Stratus Computer is also eyeing the emerging CIM market. The Natick, Mass., company has embarked on a major effort to increase the number of manufacturing packages it offers. This effort includes working with software companies to develop products for industrial production and for implementing MAP. "Manufacturing organizations are becoming aware of the need for fault-tolerant systems," says Stratus president William Foster.

Despite the attractions of the factory market, fault-tolerant-systems companies could find selling to manufacturers a very different experience. Foster says that news moves quickly in the financial community; making a sale to one broker opens the door to others. From Stratus's standpoint, 11-year-old Tandem had already established a base in that business when Stratus entered. But manufacturing is a virgin market and, Foster says, much more diffuse.

What may give all the fault-tolerant-computer makers a boost is the appearance of IBM. Big Blue entered the market earlier this year through an arrangement under which it buys and then repackages Stratus machines. The IBM machines, dubbed System 88, were sold originally on a limited basis, but the company recently announced a full-scale marketing effort under which it will sell the system nationally. Stratus projects that sales to IBM will account for 40% of its volume by 1988.

But the IBM connection could be a two-edged sword for Stratus, putting pressure on it to divert

TWO COMPANIES DOMINATE FAULT-TOLERANT SYSTEMS



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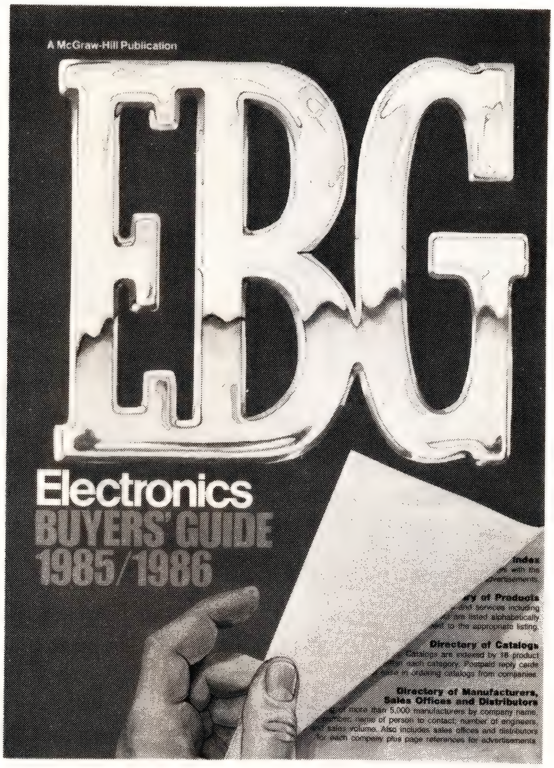
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delicate analog circuits with different components. "The problem in manufacturing analog circuits is that they are very sensitive to component variation," says McGregor. "With this package, designers can explore the effects of randomly varying components within certain tolerance ranges. These packages have been around for a while, but for use on mainframes. And they required you to be an expert user, so they weren't used. This is the first package that is actually easy enough to use."

Such attention to detail and an innovative concept have already attracted the interest of large work-station vendors to the 50-employee company. In mid-October, Analog Design Tools announced an agreement with HP under which HP's direct sales force would market Analog Workbench software for the HP 9000 Series 300 engineering work stations. It was one of four third-party software packages—and the only analog package—that HP selected. Miller adds that major Japanese chip companies, including Fujitsu, Matsushita, and NEC, have purchased Workbench products.

> *'They're addressing a powerful new sector of the market'*

Digital Equipment Corp. is also "very interested" in the product for its MicroVax II work station, according to marketing vice president Michael Carroll. Carroll says DEC has also been "in initial discussions with IBM [Corp.]" for its upcoming work-station product line.

NOT WORRIED. Daisy Systems Inc. and Valid Logic Systems Inc., the two largest digital-CAE vendors, recently announced plans to market analog software as well. But Analog Design Tools isn't too concerned. "Companies like Daisy and Valid have a large digital base and are only addressing their designers' peripheral analog needs," McGregor says. "However, since we are completely focused on the analog market, we have a good year's jump on them in terms of technology." Although Analog Design Tools considers Daisy a competitor, Dataquest's Spadarella says it is possible that the company may eventually want to connect with whatever Daisy offers.

"If they're porting their software to the popular platform work stations [such as Sun, Apollo, and MicroVax], they're addressing a very powerful new sector of the market. It's a sure-win thing," according to Bob Olton, managing analyst at Gnostic Concepts Inc., San Mateo, Calif. "The fact that IBM is even talking to them means they are privileged." *–Denise Caruso*

BOTTOM LINES

ALLEN-BRADLEY BUYS LAN, BAR-CODE UNITS

Allen-Bradley Co., the Milwaukee supplier of industrial-automation controls and electronic components, plans to acquire two businesses—a local-area-network division from 3M Co. and a bar-code-scanner unit from Scope Inc.

The Rockwell International Corp. subsidiary has agreed to buy the Interactive Systems business unit of 3M's Telecomm Division. Terms of the deal were not disclosed. Interactive Systems, which designs, installs, and supplies LANs, employs 61 people at its Ann Arbor, Mich., facility. Interactive Systems will become part of the Communications Division of Allen-Bradley's Industrial Computer Group.

Allen-Bradley has also agreed in principle to buy Scope's bar-code-scanner business. The Reston, Va., company is a subsidiary of Lexicon Corp. Terms of this agreement also were not disclosed. Scope produces laser-based bar-code scanners for industrial-automation applications, and markets them in the U. S. and Europe. Its bar-code business will become part of the Sensing Products Business Unit of Allen-Bradley's Industrial Control Division.

MICRORIM GETS ADDITIONAL FINANCING

Microrim Inc., the Bellevue, Wash., developer of data-base-management software for personal computers, has received $5 million in new equity financing. The company, which produces the software packages R:base 4000, R:base 5000, and Clout, will use the new funds for working capital, research and development on next-generation products, and marketing efforts.

GOLD HILL COMPUTERS RAISES $1.2 MILLION

Gold Hill Computers Inc., developer of Golden Common Lisp, an artificial-intelligence development and training tool, raised $1.2 million in its second round of venture financing. The Cambridge, Mass., company will use the funds to increase its research and development staff and to expand its marketing and sales department.

ALLIED-SIGNAL TO BUY OAK INDUSTRIES UNIT

Allied-Signal Inc., Morris Township, N. J., has agreed in principle to buy the Materials Group of Oak Industries Inc., San Diego, for $160 million. The Materials Group, which produces laminates and related products used to make printed-circuit boards, had 1984 sales of $186 million. At the same time, Allied-Signal says it will invest $15 million in Oak Industries and will nominate three of Oak's seven directors. The acquisition will expand Allied-Signal's product base for the electronics industry. Allied-Signal says its Norplex Division also makes pc-board materials.

OPTIGRAPHICS RAISES $7.5 MILLION

Optigraphics Corp., San Diego, has raised $7.5 million in its third round of venture financing. The company, which was founded in October 1982, makes computerized scanning and drawing-conversion systems for use in computer-aided-design and -manufacturing systems. Its Optigraphics 3000 Scanning and Conversion System has been on the market since January.

OPTOTECH ATTRACTS $6 MILLION IN FUNDING

Optotech Inc., a maker of 5¼-in. optical-disk drives, has raised $6 million in additional venture financing. The new money will be used to complete production facilities in the U. S. and the Far East, as well as for continued research and development, according to the Colorado Springs company. Optotech makes a write-once, read-mostly storage system with a capacity of 400 megabytes, designed to be integrated into systems by original-equipment manufacturers.

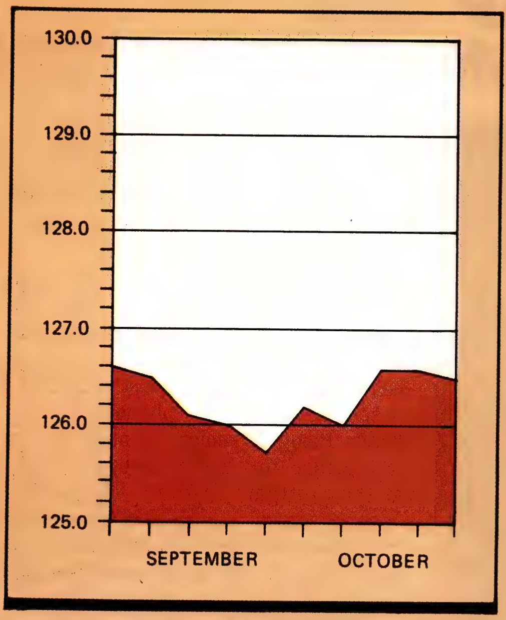
NETI TECHNOLOGIES BUYS SOFTWARE FIRM

Network Technologies Inc., Ann Arbor, Mich., has agreed to acquire Participation Systems Inc., a privately held company in Winchester, Mass., for $3.25 million in stock. Network Technologies is a subsidiary of NETI Technologies Inc., Vancouver, B. C. Both companies develop and market computer-conferencing software with which personal computer users communicate from their terminals.

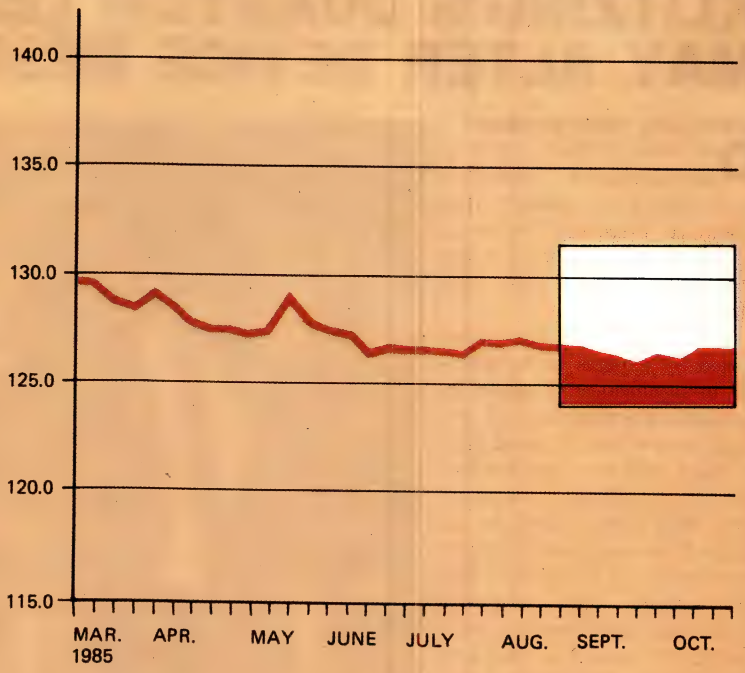
AMETEK PURCHASES HOUSTON INSTRUMENT

Ametek Inc., New York, has completed its previously announced purchase of Houston Instruments, Austin, Texas, from Bausch & Lomb Inc., Rochester, N. Y., for $46 million. Ametek says Houston Instruments will continue operations as a division of Ametek. Houston Instruments makes graphic plotters and digitizers used in computer-aided design and -manufacturing operations.

ELECTRONICS INDEX



THIS WEEK = 126.5
LAST WEEK = 126.6
YEAR AGO = 131.5
1982 = 100.0



The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. ELECTRONICS SHIPMENTS

Shipments ($ billions)	September 1985	August 1985	September 1984
Communications equipment	5.507	5.287	4.749
Radio and TV receiving equipment	0.886	0.894	0.854
Electronic and electrical instruments	4.542	4.706	4.540
Components	3.047	3.212	3.946

U. S. GENERAL ECONOMIC INDICATORS

	September 1985	August 1985	September 1984
Index of leading economic indicators	170.3	170.2	165.7
Budgeted outlays of the federal government ($ billions)	73.191	83.621	51.234
Budgeted outlays of the Department of Defense ($ billions)	21.498	23.209	18.942
Operating rate of all industries (% capacity)	78.3	78.5	80.1
Industrial-production index	124.7	124.8	123.3
Total housing starts (annual rate in thousands)	1,583	1,746	1,669

A 0.8% drop in shipments of electronic equipment in September pushed the *Electronics* Index deeper into its slump. The month's declines brought shipments by the U. S. electronics industry down to a level nearly 1% lower than those of a year ago.

Nonetheless, one industry segment—communications equipment—managed to show some strength. Shipments in this sector rose 4.2% in September, bringing shipments up 16% above last September's levels. Unfortunately, the rise in communications equipment was canceled out by the month's 5.1% decline in shipments of components. Shipments in this segment were down 22.8% over the same period last year.

Relief from the doldrums in which the electronics industry finds itself is not yet on the horizon. As exhibited by an inconsequential rise in leading general economic indicators, the overall economy has slipped into a lethargic state. Though the U. S. gross national product experienced a generous 3.3% rise in the third quarter, the only real strength in the economy was in government spending.

for the ohm could be adopted worldwide as early as next year, Ploog says.

Klitzing carried out the crucial measurements that led to his discovery at the High Magnetic Field Laboratory in Grenoble, France, a facility run jointly by the Stuttgart Institute and France's Centre National de Recherche Scientifique. But, as is often the case in the history of discoveries, the German physicist was originally after something other than what he found.

Klitzing wanted to investigate the extent to which the electrical characteristics of semiconductor crystals depend on the various factors, including impurities, that are involved in their fabrication. In other words, he was out to shed light on what physicists call the "dirt effects" related to the impurities in a semiconductor material.

Investigating the 'dirt effects' led to the discovery

What he found, however, was something very different—pronounced horizontal sections in the material's resistance curves. These plateaus, he discovered, do not depend on the amount of impurities at all; nor do they have anything to do with the sample's dimensions. What Klitzing had hit upon was a new elementary phenomenon: the quantum Hall effect, or, as his colleagues call it, the Klitzing effect—one based on fundamental constants.

The tousle-haired, boyish-looking 42-year-old recalls exactly when he confirmed that the resistance plateaus are determined solely by fundamental physical constants. "It was on Tuesday, the fifth of February 1980, at 2 o'clock in the morning," he says. (The big Grenoble magnet he worked with consumes so much power that it can be operated only during the night when the other magnets are shut down.)

The astounding thing about the discovery of the quantum Hall effect is how little technical equipment was involved, Klitzing's colleagues point out. Though the breakthrough came only with the aid of a strong magnetic field exhibiting 20 Tesla, or 200,000 gauss, which is equivalent to about 400,000 times the earth's magnetic field, at the heart of the experiments were simple FET samples a little bigger than commercial types.

As Hans Queisser, also a director at the Stuttgart Institute, puts it, "One of the most exciting developments in physics today was carried out not in those expensive, kilometer-long tunnels that high-energy physicists use but in the interior of a crystal."

That is fitting, because Klitzing is a practical type who at one point wanted to work in industry. That came after he studied physics at the Technical University of Braunschweig and acquired a doctoral degree in 1972 at the University of Würzburg. Following research work at Oxford University, he qualified as a lecturer at Würzburg in 1978.

His career in pure research might have ended right then ("I had already looked for a position in the industry," he says) had not the German Research Society and the Max Planck Society initiated a program aimed at advancing promising young scientists in their specialties.

Under a scholarship, Klitzing pursued his "dirt effect" investigations. But at only 14.6 T, the magnet available at the university there was too weak for the discovery he made eventually. That changed when Klitzing went to work as a "guest researcher" at Grenoble in August 1979. In winter 1980, it took him only two weeks to carry out his epochal measurements.

Klitzing's original intent was to study the interfaces of MOS FET samples by looking into the behavior of electrons under extreme conditions. In a MOS FET, the electrons are squeezed into a thin channel right below the surface by means of a voltage applied to the gate—that is, by an electric field. This field, which is arranged perpendicularly to the two-dimensional electron "gas," considerably restricts the electron motion in the channel.

Klitzing then subjected the electrons to a strong magnetic field. This further constrained the motion of electrons in the channel, allowing them to travel only along tiny circular paths. The samples were kept at a temperature of less than 4 K to eliminate most of the resistance to electric conduction.

Hall resistance can be independent of applied magnetic field

The quantum Hall effect showing up under these conditions manifests itself most drastically in transport quantities such as the so-called Hall resistance—the ratio of the transverse voltage to the current. In a three-dimensional sample, the Hall resistance is proportional to the applied magnetic field.

But in a 2-d sample, the resistance curve plotted against the field looks like a staircase, with the horizontal part of each step forming the aforementioned plateau. This means that within certain ranges, the Hall resistance is independent of the applied magnetic field. *–John Gosch*

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file-server unit. Ordinarily, Microsoft's Networks requires the server to be dedicated to network operations, and it cannot accommodate a local user. The redirector and DOS 3.1 provide strong capabilities for third-party vendors, Buchanan says.

He adds that while 3Com has no joint development efforts going on with Microsoft, the two companies have cooperated in selling products.

The 3+ series will be available in January through 3Com's dealers. Products are sold as single or double modules; the single version will support up to five users and the double an essentially unlimited number—though the practical limit may be 20 or 30, according to the company.

The Share module sells for $550 per network server, the Mail module for $250, Route for $1,250, and Path, the upgrade module, for $500. 3+ Remote costs $295 per work station.

3Com Corp., 1365 Shorebird Way, Mountain View, Calif. 94043. Phone (415) 961-9602 [Circle reader service number 338]

$85,000 SYSTEM CHECKS 512 TEST POINTS

Zehntel is set to announce an in-circuit tester that it claims will crack the market for low-cost board testers wide open. The Zehntel 875 will carry a price tag of $85,000—about half that of the Zehntel 850 tester, which has similar capabilities [*Electronics,* Oct. 6, 1983, p. 254].

A key feature of the unit, which will be unveiled Nov. 19 at the International Test Conference in Philadelphia, is its ability to perform extensive analog and digital testing, says Koorosh Nazifi, the company's product marketing manager. A programmable pattern-sequence generator is provided for checking test points on boards populated with up to 512 large-scale and very large-scale ICs. A 16-bit analog test module that is program- and language-compatible with the Zehntel 850 permits six-wire measurement testing, transistor beta testing, parallel RC measurement, and mixed-signal testing capability for hybrid devices such as codecs. An optional amplifier permits up to 100-V ac stimuli for high-voltage equipment.

Like the other in-circuit test systems in the Zehntel 800 series, the 875 is based on AT&T's Unix operating system and uses a 32-bit 68010 microprocessor with 1 megabyte of memory, expandable to 2 megabytes. A 48-megabyte 5¼-in. Winchester disk drive is used for mass storage, and a 17½-megabyte streaming-tape cartridge is used to transfer files to other products in the 800 series.

"The major advantage that the 850 still has over the 875 is the [former's] ability to test a greater number of nodes—1,024 versus 512," says Nazifi. "This makes the 850 the tester of choice for the big manufacturers who use a lot of digital devices. But our plan for the 875 is to get it into smaller shops that wouldn't have considered an in-circuit tester before."

Zehntel is focusing its marketing efforts for the 875 on manufacturers that produce analog equipment also containing digital devices. Analog equipment can present even more serious testing challenges than digital devices, points out Craig Pynn, Zehntel's vice president of marketing. Zehntel's approach is to present the engineer with a test system that has a modular architecture—built around a general-purpose motherboard and the test modules that plug into it.

Pynn stresses that manufacturers with little previous experience with in-circuit testers can easily use the 875. A standard instructional software package called Tester-Aided Instruction is available to help users develop hands-on experience. In addition, users of popular computer-aided-engineering and -design systems can automatically create the circuit descriptions (input lists) on the 875 as a first step in test-program generation.

Up to four additional terminals for off-line editing and programming can be added with an optional serial interface package. For users with larger programming loads, the 875 can be interfaced to the Zehntel 700 Net Workstation over an Ethernet or a serial interface port. Shipments are scheduled to start next month. *–David M. Weber*

Zehntel Inc., 1600 S. Main St., Suite 320,
Walnut Creek, Calif. 94596.
Phone (415) 946-0400 [Circle 339]

ANALOG, TOO. The low-cost Zehntel 875 tests analog as well as digital ICs.

A 5-Mb/s LAN COSTS $495 PER NODE

Higher speed and lower cost mark the latest addition to the emerging market for local-area networks that are compatible with IBM Corp.'s Netbios protocols. The 5-Mb/s LAN that AST Research will unveil at next week's Comdex/Fall '85 in Las Vegas is 1 Mb/s faster than IBM's Token Ring Network.

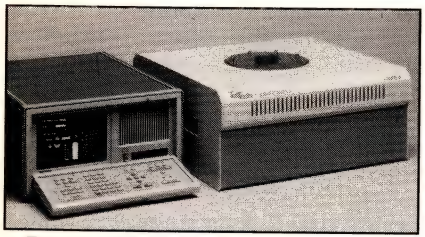
The Irvine, Calif., company's Resource Sharing Network will complement both IBM's Token Ring Network and the PC Network—but it will cost well below both at $495 per attachment. IBM's PC Network typically sells for $645 per personal computer adapter card, and its token-ring adapter card work users simultaneously.

AST will also demonstrate at the Comdex show the network version of the Knight Security Manager, which adds password protection and electronic mail to the Resource Sharing Network. The security manager sells for $395 per network. *–Robert Rosenberg*

AST Research Inc., 2121 Alton Ave., Irvine, Calif. 92714.
Phone (714) 720-1824 [Circle 340]

LOGIC-ANALYSIS TEST ADDED TO DAS 9100

Users of Tektronix' popular DAS 9100 digital analysis system now have a benchtop logic-analysis test fixture at their disposal. The TF-100 supports 320 pins and operates at up to 50 MHz.



Designed for analysis of very large-scale integrated circuits, the TF-100 comes with a removable and interchangeable device-adapter card that supports variations in package style, including a 21-by-21-pin grid array and a dual in-line package.

Eight 50-Ω coaxial paths between the fixture and the device-adapter card permit interfacing to other test and measurement instruments.

The TF-100 fixture's price, including the device-adapter card, is $5,000. Deliveries will begin this month.

Tektronix Inc., Logic Analyzer Marketing, P. O. Box 12132, Portland, Ore. 97212.
Phone (800) 245-2036; in Oregon, (503) 231-1220 [Circle 354]

UNIT RUNS ALL TESTS FOR FCC PART 68

A single rack-mountable work station designed to make electrical and environmental tests in accordance with Federal Communications Commission Part 68 specifications replaces the variety of instruments previously used. Part 68 covers compliance for any device that attaches to the telephone network.

The system's major test components handle hazardous voltages and currents, signal-power limitations, balance, impedance limitations, billing protection, and surges.

The manufacturer says the work station takes the average operator one day to learn. The product's price, $49,950,

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January
- Philips Uses MBE for Lasers
- Siemens Readies Commercial ISDN
- Japanese Chemical Firm Moves from Soap to Floppies
- Italian Firm Seeks Allies to Crack U.S.
- Japan Pursues Role in Space
- Bellman Switches on Italtel for Expansion
- Robots get Smart in Japan
- ITT Invests in European Units Crack U.S.

February
- Europe's Esprit Finally Sets Sail
- LSI Logic Counts on Sandfort to make its Mark in Europe
- Upstart Vendor Makes Waves in Japan's Robot Market
- NEC Fashions New Fab Process
- Olivetti's Viti Directs ET Designs that Marry Bus & Art
- German Startup's Success Surprises Europeans
- Britons Seek Tolerant Chips
- OBI Rains on IBM's Parade
- Mega's Friedrich Aims to Cut Asian Lead in Memories

March
- British GaAs Chips Go to Market
- NEC's CPU Leapfrogs IBM
- Hitachi CPU Challenges IBM
- France's Lansat Rival Set for Fall Launch
- Olivetti Stakes Claim in Video Typewriters
- Italian VLSI Chip has the Right Accent
- Koreans Try for VCR Replay
- Germans Push X-ray Exposure
- There's Life in Resistors, German Company Finds
- UK Beats a Path for Europe's Race

April
- German System Meets New ICAO Standard
- West Germans Squabble Over Choice of IFF
- Britain Promotes Open Architecture
- US Makes Progress in Japan Telecom Talks
- Japan's Lead in Optical Disks: It's Part of the System
- Daisenberger Guides US Firms through Red Tape
- Asia: It's No Longer Just Japan That Threatens US Markets
- Malaysia: Top Shipper of Discretes
- Indonesia: Domestic Sales are the Lure

May
- Thomson's VCR System Clears Up Doubts
- ICL Banks on Networks and Japanese Chips
- Min Blazes Bright Path for Korea's Gold Star
- Asia: The Four Dragons Rush to Play Catch-up Game
- Singapore Casts Lot with Software
- Philips' Eurom Chip Finally Debuts
- Sagging Prices Sting Japanese Producers
- British Telecom Spreads Its Wings with Mitel
- South Korean IC Maker Seeks World Markets

June
- Plessey Switches Off Flash ADC, Saves Power
- Sony Campaigns Hard for BMM Camcorders
- Japanese Quit on IBM Software, Turn to UNIX
- Apple Tries Again to Blast Off in Japan
- Has the End Come for European Chip Makers?
- SIA Protest May Not Stem Trade Tide
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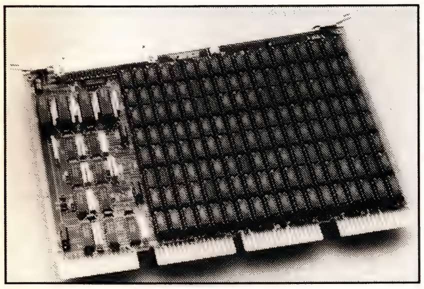
SPEEDY VME CPU RUNS WITHOUT WAIT STATES

The VMEbus CPU-21 makes use of Motorola Corp.'s 68020 microprocessor and 68881 floating-point coprocessor to run at 16.7 MHz without wait states. It addresses as much as 1 megabyte of high-speed local static RAM. A fully configured system includes up to 512-K bytes of 32-bit-wide EPROM, a VMXbus interface, and two serial I/O channels.

One channel is a debug port. The other is an all-purpose interface for a printer or host connection, eliminating any need for a separate RS-232-C board. A second board, the CPU-20, comes without the 68881. Prices for the CPU-21 start at $5,450; delivery takes 30 days.

Force Computers Inc., 727 University Ave.,
Los Gatos, Calif. 95030.
Phone (408) 354-3410 [Circle 372]

MICROVAX II CARD PACKS 4 MEGABYTES



The NS630, a quad-wide memory card for Digital Equipment Corp.'s MicroVax II, has up to 4 megabytes of RAM and permits memory to be electrically removed from the system without physically removing it from the backplane. All RAMs are socketed and an additional burned-in RAM, located on-board to aid field servicing, is included. The card is equipped with an on-line/off-line switch with LED indicator.

The NS630 sells for $2,765 and is available now.

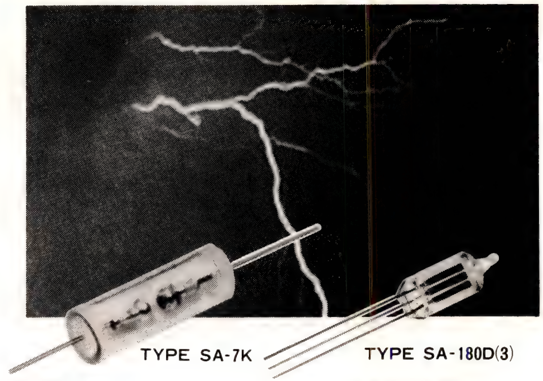
National Semiconductor Corp., 2900 Semiconductor Dr., P. O. Box 58090, Santa Clara, Calif. 95052. Phone (800) 538-8510; in California, (408) 721-5000 [Circle 370]

EXPANSION BOARD BOOSTS PC's MEMORY

Conquest, an expansion board for the IBM Corp. Personal Computer, the IBM PC/XT, and compatibles, replaces up to three standard expansion boards. This multifunction board is intended mainly to expand memory in large spreadsheet programs.

Conquest features the Lotus-Intel-Microsoft expanded-memory specifications. PC Network local-area-network adapter

SURGE FREE SURGE ABSORBABLE DISCHARGE TUBE FOR CIRCUIT PROTECTION



● TYPE

Type	Breakdown Voltage (V) DC	Insulation Resistance (Ω)	Maximum Surge Current (8 × 20us) KA	Life Times at 500A
SA-80SS	80 ± 10%	10^{10} min	1.0	1000
SA-200SS	200 ± 10%	10^{10} min	1.0	1000
SA-80	80 ± 10%	10^{10} min	1.5	1000
SA-140	140 ± 10%	10^{10} min	1.5	1000
SA-200	200 ± 10%	10^{10} min	1.5	1000
SA-250	250 ± 10%	10^{10} min	1.5	1000
SA-300	300 ± 10%	10^{10} min	1.5	1000
SA-7K	7000 ± 1000V	10^{10} min	—	5000
SA-10K	10000 ± 1000V	10^{10} min	—	5000
SA-180D(3)	180 ± 10%	10^{10} min	2.5	1000

SA-180D(3) is a three electrode discharge tube.
All tubes can be made dark effect redused types which are available upon request. D is added to the model number, as in SA-80DSS.

● POINT

(1)Usable at wider ambient condition, especially good under high humidity.
(2)Visibility for operation.
(3)Compact and easy assembly.
(4)Stable characteristics.

● APPLICATION

Computer circuit.
Communication equipment.
Home Appliance.
Aircraft and Automobiles.

MAIN PRODUCT NEON GLOW LAMP, XENON FLASH LAMP, RARE GAS DISCHARGE LAMP
MINIATURE: BLACK-LIGHT, UV-LIGHT, FLUORESCENT COLOR-LIGHT

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circuitry is optional. The board sells for $395 with sockets that provide a 2-megabyte capacity but without installed RAM. A chip set containing nine 256-K 150-ns RAMs for Conquest sells for $95.

Orchid Technology, 47790 Westinghouse Dr., Fremont, Calif. 94539.
Phone (415) 490-8586 [Circle 369]

INTERNAL TAPE KIT BACKS IBM PC DISKS

InnerSpace IT60 is an internal tape backup kit for the IBM Corp. Personal Computer and compatibles. The streaming-tape cartridge drive operates at the rate of 90-K bytes per second and archives the contents of a 60-megabyte disk in less than 15 minutes.

Installing the 5¼-in. half-height, internally mounted drive takes less than 10 minutes, the manufacturer says. The package, which includes the tape and controller, sells for $1,595 and is available now for immediate delivery.

Priam Corp., 20 W. Montague Expwy., San Jose, Calif. 95134.
Phone (408) 946-4600 [Circle 377]

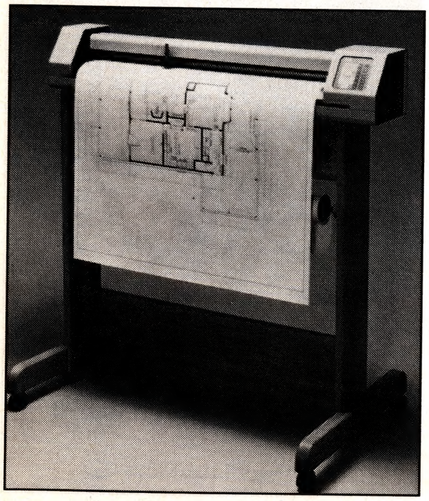
PLOTTER TAKES 37½-BY-80-IN. PAPER

The LP 3700 plotter enables users to plot on a range of paper sizes, including 37½-by-80-in. size E sheets. Users can plot on any size medium—either sheet or roll stock. The plotter is designed for use with computer-aided-design systems built around personal computers.

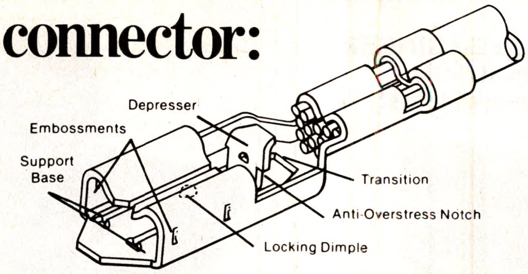
The LP 3700 has ±0.0025-in. plotting resolution. Plotting speed is selectable from 1 to 10 axial in./s. Standard RS-232-C interfacing makes it compatible with most host-computer hardware.

Delivery of the LP 3700, which costs $4,995, is from stock.

Ioline Corp., 19417 36th Ave. W., Suite D1, Lynnwood, Wash. 98036.
Phone (206) 775-7861 [Circle 376]



AMP positive-lock connector:



It joins a blind mate with a click.

You know it's locked and safe even under severe vibration. This positive-lock connector offers other important benefits, too. Low insertion force. Mates with NEMA DC-2 tabs with holes. Can be terminated by hand, or automatic tools. Sizes to fit 22-18 AWG and 18-14 AWG wires.

For more information, complete and return this card. Or call the AMP Positive-Lock Information Desk at (717) 780-4400.

AMP Interconnecting ideas.

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Wiltron is Europe.

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Wiltron has been solving Europe's unique measurement problems for the past 25 years. Working with defense ministries to better test crucial signal paths in planes and ships. And helping major electronic manufacturers with their specialized measurement needs.

When the U.K. government awarded its first ever R&D grant to a foreign firm, it went to Wiltron. Now, European developed products are being manufactured in a new Wiltron plant outside of London. European technology for European markets.

It's all part of staying close to customer needs... with direct offices and distributors throughout Western Europe. Call Wiltron at 408-778-2000.

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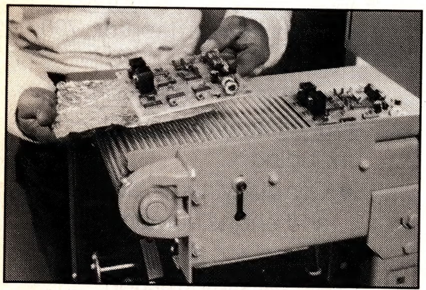
one can of compressed gas and the valve assembly sells for $25.

Texwipe Co., P. O. Box 575, Upper Saddle River, N. J. 07458.
Phone (201) 327-9100 [Circle 426]

EPOXY RESIN. A one-component epoxy resin for pc boards offers a glass-transition temperature higher than 180°C, which makes it more dimensionally stable than polyimide. The manufacturer says its resin, Quatrex 5010, is a trisphenol-based system competing in the high end of single- and multilayer-board markets, where processing and use temperatures are elevated. Quatrex 5010 also offers good moisture and blister resistance and minimizes drill smear. Full cure is reached in 2 hours.

Dow Chemical Co., Midland, Mich. 48640.
Phone (517) 636-0273 [Circle 427]



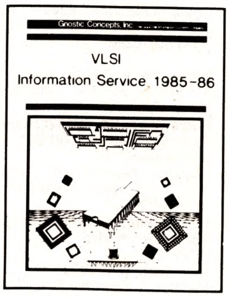
CONFORMAL COATING. Shadowcure 361 conformal coating cures in 6 to 20 seconds under ultraviolet light, depositing a protective film 1 to 3 mils thick on pc boards. In shadow areas the lamp can't reach, proprietary chemistry cures the coating in 24 to 48 hours. The acrylic and urethane hybrid meets MIL-I-46058C standards and is thin enough to be sprayed onto boards in high-speed assembly lines. Existing spray-coating lines can be modified easily to accept Shadowcure 361. Initial coating and curing time for a single board is less than 1 minute.

Loctite Corp., Shadowcure Process Center, 705 N. Mountain Rd., Newington, Conn. 06111. Phone (203) 246-1223 [Circle 428]

ADHESIVE. Aremco-Bond 614 is a nickel-epoxy adhesive offered as a low-cost substitute for silver epoxies. The two-component material possesses excellent adherence to metals, ceramics, and many plastics, the manufacturer says. It is used in applications where conventional solders do not work, such as attaching a copper lead to a ceramic substrate. Aremco-Bond 614 also bonds electromagnetic- and radio-frequency-interference shielding to form a conductive path.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562.
Phone (914) 762-0685 [Circle 430]

STRENGTH THROUGH KNOWLEDGE



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LETTERS

Video-disk storage

To the editor: Contrary to what is stated in "Optical Storage: Hot Item or Dud?" [*Electronics*, Sept. 16, 1985, p. 26], our S2000 12-in. video disk stores 1 gigabyte of user information. The comparison with our series 500 CDROM is misleading because the S2000 is a computer peripheral with an average access of 150 ms, versus 0.5 to 1 s on the CDROM.

James H. Kelly
Vice president, optical disk operations
Reference Technology Inc.
Boulder, Colo.

Not Sony alone

To the editor: "TV Projector Makers Shift Aim to Business" [*Electronics*, Oct. 7, 1985, p. 19] contains incorrect information about Electrohome Ltd.

First, the Electrohome ECP 2000 does offer automatic scanning; it automatically locks onto terminal scan signals from 15 to 33 KHz horizontal and 45 to 100 Hz vertical—the same statistics as the Sony VPH-1030Q1—as did the Electrohome ECP1000, introduced in 1983.

Also, unlike other manufacturers, Electrohome has not shifted to the data and graphics market but started there with the EDP56 monochrome projector in 1979. Our first color projection system, the ECP 1000, was designed as a computer projector. We do not share the thoughts of Raymond Boggs of Venture Development Corp. that there may not be a strong market for these devices. On the contrary, we have seen this product evolve from a business toy to a well-accepted business tool.

Tom Sutherland
Marketing manager, projection products
Electrohome Ltd.
Kitchener, Ontario, Canada

Wrong source

To the editor: "Work stations gain supercomputer strength" [*Electronics*, Sept. 30, 1985, p. 52] gives the wrong source for the 10,000-gate CMOS gate arrays that Mentor Graphics Corp. uses to build processor circuits. The gate arrays are from LSI Logic Corp.

Di Schwartz
Manager, marketing communications
LSI Logic Corp.
Milpitas, Calif.

Correction

"Hitachi and Motorola Team Up for CMOS 68000," [*Electronics*, Sept. 23, 1985, p. 12] should have listed Motorola's 16-bit 68HC000 processor as being pin-for-pin compatible with the n-MOS 68000.

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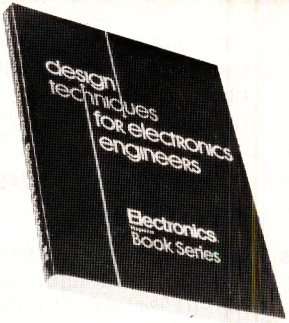

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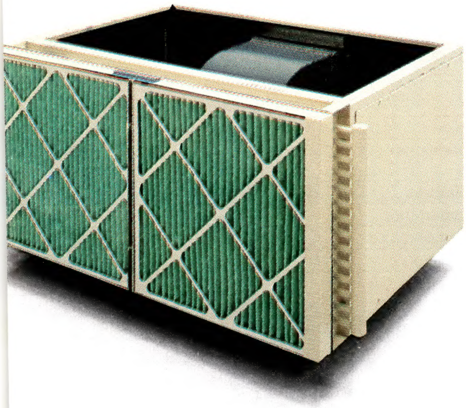

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